Advantech

SOM-Express
System On Module

Design Guide

Version 1.1

Your ePlatform Partner

ADVANTECH

Notices

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Revision History

Version/Revision date	Date	Description
Version 1.0	July, 2006	Initial release
Version 1.1	July, 2007	

Part No: 20060EXP00

Table of Contents

Chapter 1 Introduction

This design guide organizes and provides Advantech's SOM carrier board design recommendations for Advantech SOM-Express modules. It specifies common mechanical and electrical characteristics in order to ensure the carrier board design meets all the requirements needed to work properly.

1.1 Terminology

Table 1.1 Conventions and Terminology	
AC'97	Audio Codec 97'
AGP	Accelerated Graphics port refers to the AGP/PCI interface
CPU	Central processing Unit
CRT	Cathode Ray Tube
DDR2	Double Data Rate second generation SDRAM memory technology
DTOS	Advantech's Design To Order Service
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
SOM-Express	New generation technology of System on module
FSB	Front Side Bus, synonymous with Host or CPU bus
GMCH	Refers to the Graphics Memory Controller Hub chipset component
I2C	Inter-IC (a two wire serial bus created by Philips)
ISA	International Standards Association
IDE (ATA)	Integrated Drive Electronics (Advanced Technology Attachment)
INTx	An interrupt request signal where x stands for interrupts A, B, C, and D.
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential Signaling: A high speed, low power data transmission standard used for display connections to LCD panels.
MCH	Refers to the Memory Controller Hub chipset component
NTSC	National Television Standards Committee
PAL	Phase Alternate Line
PCI	Peripheral Component Interface
PCI-Express	New generation PCI interface with serial interconnection technology
RTC	Real Time Clock
SMBus	System Management Bus.
SOM	System On Module
SATA	Serial ATA interface
SAS	Serial attached SCSI interface
ULV	Ultra-Low Voltage
USB	Universal Serial Bus

1.2 Referenced Documents

Table 1.2 Referenced Documents

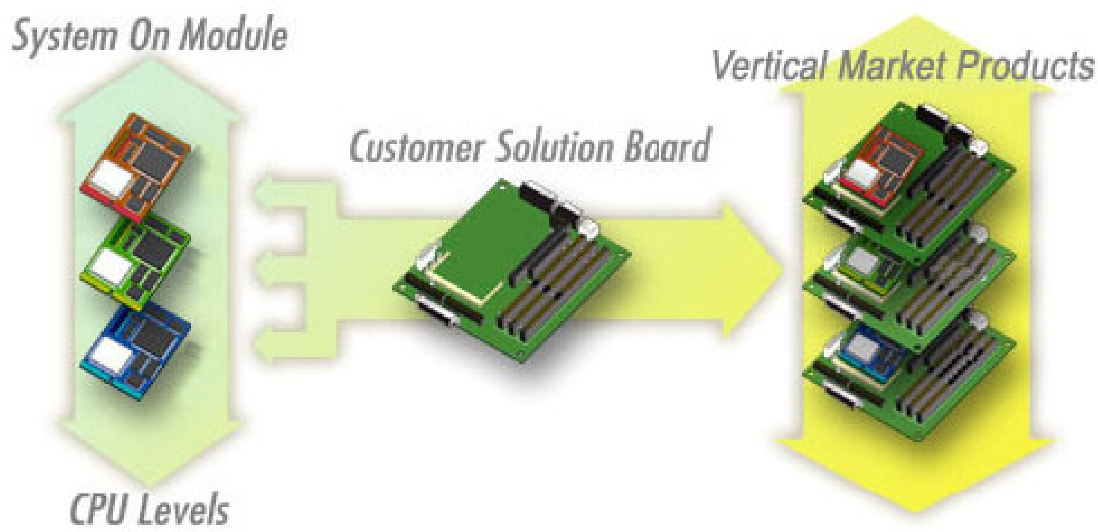
Document	Location
Advanced Configuration and Power Management (ACPI) Specification 3.0b	http://www.acpi.info/spec.htm
COM Express Specification	http://www.picmg.org/
Ethernet(IEEE 802.3)	http://www.ieee.org/portal/site
I2C Bus Interface	http://www.semiconductors.philips.com/
IrDA	http://www.irda.org/
PCI	http://www.pcisig.com/
PC104	http://www.pc104.org/technology/pc104_tech.html
RS232	http://www.eia.org/
SMBus	http://www.smbus.org/specs/
USB	http://www.usb.org/home

Chapter 2 SOM-Express Overview

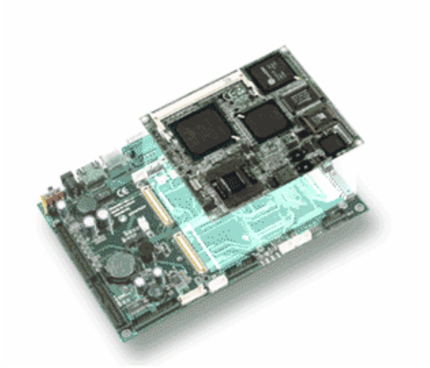
SOM-Express complies with COM Express standard from the PCI Industrial Computer Manufacturers Group (PICMG) which provides next generation performance of the smallest state of the art embedded modules. With a scalable solution that meets customer's advanced CPU application development needs and reduces time-to-market. Advantech's Design To Order Service (DTOS) helps customers develop custom CPU board solutions extremely fast and with lower investment. With DTOS, three ready-to-run engineering samples can be produced within 30 working days from order confirmation. Using SOM-DTOS, customers can reduce traditional customized CPU board development time and costs by as much as 80%.

2.1 Overview

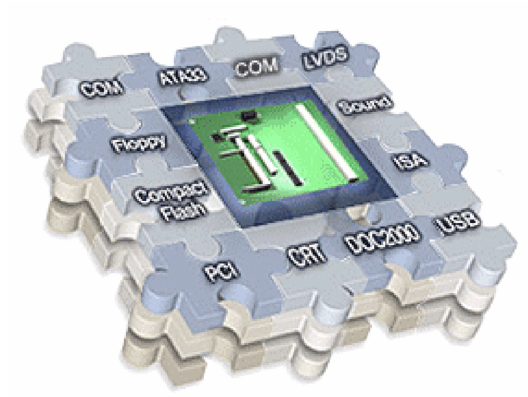
Advantech offers a wide range of SOM products to cater to each customer's demands. The modular designs allow upgrade ability and add more flexibility to the system. The COM Express form factor allows the SOM-Express modules to be easily and securely mounted on a customized solution board. The design and multiple processor choices eliminate CPU integration worries and allow fast application support for the most dynamic embedded needs.



SOM is a series of reliable and widely used CPU cores with high integration features. SOM-Express supports wild range of processor and chipset solution available from the market to reach the latest technical trend such like PCI Express, Serial ATA, USB 2.0, etc. Not only does SOM allow quick design, it also provides the benefits of easy installation, maintenance and upgrade ease.



Though small in size, SOM takes care of most complicated CPU architectures and basic common circuits. Many system integrators are finding an Advantech SOM solution already covers 80% of their feature requirements. This makes SOM a powerful time and money saver.



SOM + Customer Solution Board = Your Customized Platform. System On Modules save time and money. Using SOM-DTOS allows customers to realize cost savings and most importantly, faster time to market, two keys to help ensure your product's success in the market.

2.2 Specifications

Advantech provides two SOM-Express modules, and each module has a different CPU type for customer to choose. Table 2.1 shows Advantech SOM-Express modules with brief descriptions.

Table 2.1 SOM-Express Module	
SOM-5780 Series	**Description**
SOM-5780FL-00A1E	Socket 478 Type
SOM-5780FL-S0A1E	On board Intel Celeron M ULV 373 @ 1.0G
SOM-5780FL-S4A1E	On board Intel Pentium M LV 738 @ 1.4G
SOM-5780FL-S8A1E	With Intel Pentium M 745 @ 1.8G
SOM-5780FL-U0A1E	With Intel Pentium M 760 @ 2.0G
SOM-5782 Series	**Description**
SOM-5782FL-00A1E	Socket 478 Type
SOM-5782FL-S0A1E	On board Intel Celeron M ULV 423 @ 1.06G
SOM-5782FL-S7A1E	On board Intel Core Duo L2400 @ 1.66G
SOM-5782FL-U0A1E	With Intel Core Duo T2500 @ 2.0G
SOM-DB5700	**Description**
SOM-DB5700-00A1E	SOM Express Development Board Rev.A1

2.2.1 SOM-5780

Advantech's new SOM-5780 is the ultimate powerful SOM-Express CPU module able to drive the most demanding embedded applications requiring high performance CPU processing power & graphics support. With support for Intel® Pentium® M and Celeron® M processors & enhanced SpeedStep technology, the SOM-5780 offers developers a low power and scaleable solution that fits a range of needs. The Intel® 915GM Express Chipset for Embedded Computing, consisting of the Intel 915GM Graphic Memory Controller Hub (GMCH) and Intel I/O Controller Hub 6-M (ICH6-M) is an optimized integrated graphics solution with a 400MHz and 533MHz front-side bus. The integrated 32-bit 3D graphics engine, based on Intel Graphics Media Accelerator 900(Intel GMA 900) architecture, operates at core speeds of up to 320MHz. It features a low-power design, is validated with the Intel Pentium M and Intel Celeron M processors on 90nm process, and supports up to 2GB of DDR2 533MHz system memory.

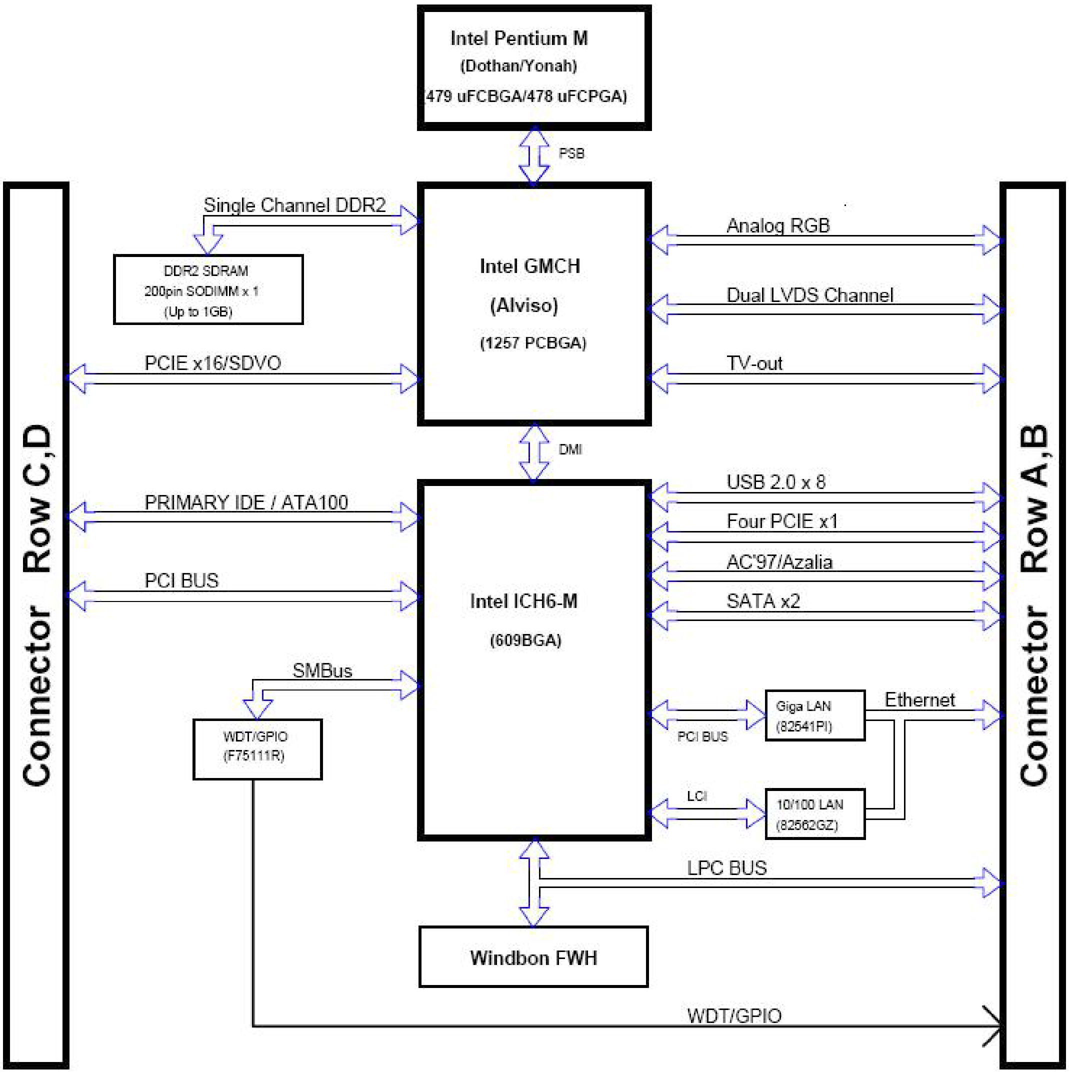


Figure 2-1 SOM-5780 Block Diagram

SOM-5780 Main Features:

Embedded Intel® Pentium® M/ Celeron M processor
Intel Extreme Graphics 2 & PCI Express graphics
Supports the upcoming primary datapath PCI Express
Supports 8 host USB2.0 ports and 4 SATA
Supports up to dual channel LVDS panels

Table 2.2 SOM-5780 Specifications

Item	Description
CPU	Embedded Intel Pentium M or Celeron M processor w/64KB primary cache memory
System Memory	1 x 200 pin SO-DIMM sockets, support Double DataRate2 (DDR2)128 MB to 1 GB, accept 128/256/512/ 1000 MB DR200/266/333 DRAM.
2nd Cache Memory	2/1 MB on the Pentium M processor or 512 KB on the Celeron M processor.
System Chipset	Intel 915GM GMCH/ ICH6-M Chipset 533 MHz FSB
BIOS	AWARD 4 Mbit Flash BIOS
WatchDog Timer	255 levels timer interval, from 1 to 255 sec or min setup by software, jumperless selection, generates system reset
Expansion Interface	Support PCI Express, PCI & LPC interface
MIO	1 x EIDE (UDMA 100), 2 x SATA
USB	8 USB 2.0 compliant ports
Ethernet	Intel 82562GZ, IEEE 802.3u 10/100Base-T compatible Built-in boot ROM in Flash BIOS Optional Intel 81541PI IEEE 802.3u 1000Base-T compatible
CRT Display mode	Pixel resolution up to 1600 x 1200 at 85 Hz and 2048 x 1536 at 75 Hz
LCD Display mode	Dual channel LVDS panel supports up to UXGA panel resolution with frequency range from 25 MHz to 112 MHz
Dimensions (L x W)	95 x 125 (3.74" x 4.92")
Power Supply Voltage	+12 V power only
Power Requirement	Max: +12 V @ 4 A
Operating Temperature	0 ~ 60˚ C (32 ~ 140˚ F)
Operating Humidity	0% ~ 90% relative humidity, non-condensing

2.2.2 SOM-5782

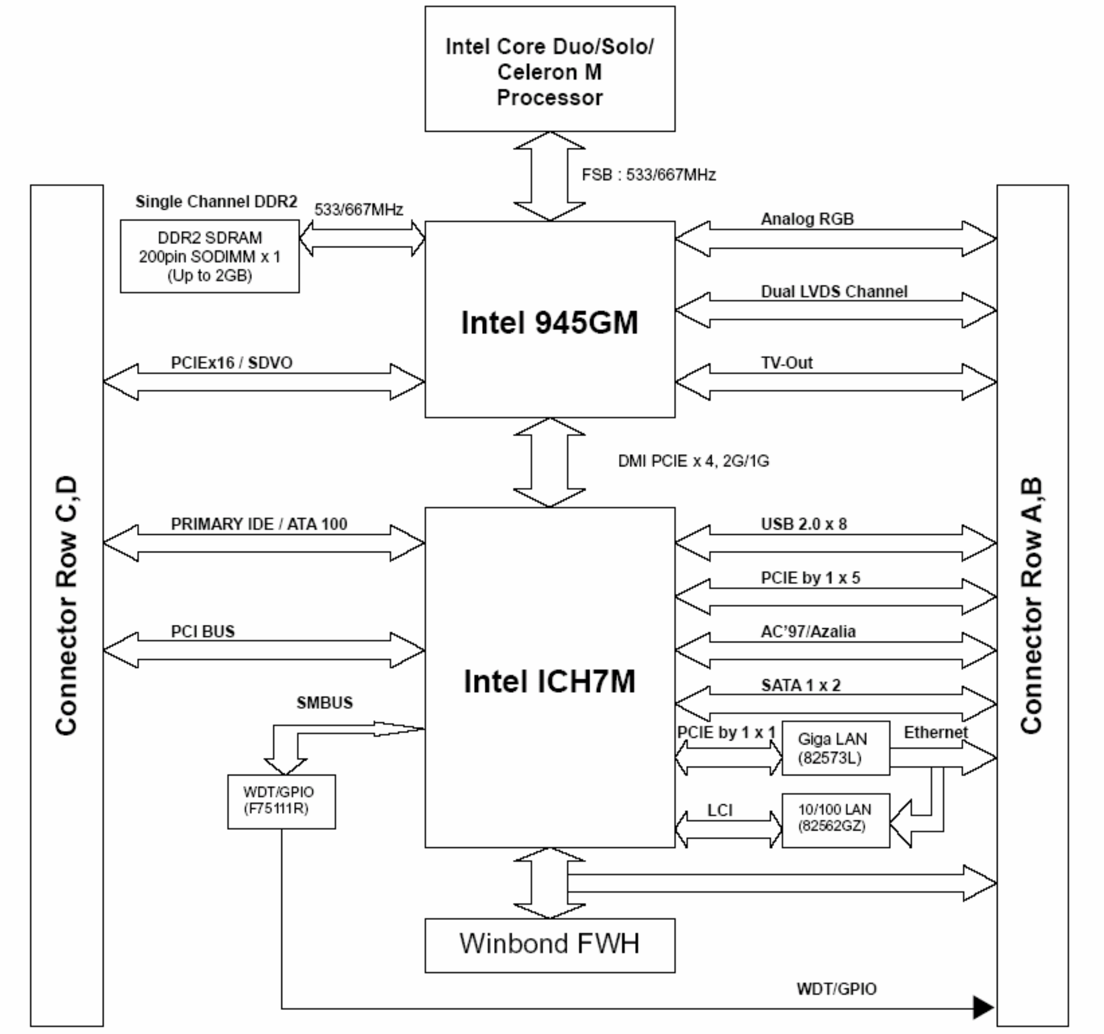


Figure 2-2 SOM-5782 Block Diagram

SOM-5782 Main Features:

- Embedded Intel® Core™2 Duo / Core™ Duo / Celeron® M Processor
- Intel new graphics core based on GMA 950 & external PCI Express x 16 graphics interface.
- Supports the upcoming primary datapath PCI Express
- Supports 8 host USB 2.0 ports and 2 SATA ports
- Supports up to dual channel LVDS panels

Table 2.2 SOM-5782 Specifications

Item	Description
CPU	Embedded Intel Intel Core 2 Duo processor / Intel Core Duo processor, Intel Core Duo processor LV (Low Voltage).
System Memory	1 x 200 pin SO-DIMM sockets, support Double Data Rate2 (DDR2)128 MB to 2GB, accept 128/256/512/1024/2048 MB DDR 533/667 DRAM.
2nd Cache Memory	2-MB L2 cache
System Chipset	Intel 945GM GMCH/ ICH7-M Chipset 533 MHz FSB
BIOS	AWARD 4 Mbit Flash BIOS
WatchDog Timer	255 levels timer interval, from 1 to 255 sec or min setup by software, jumperless selection, generates system reset
Expansion Interface	Support PCI Express, PCI & LPC interface
MIO	1 x EIDE (UDMA 100), 2x SATA
USB	8 USB 2.0 compliant ports
Ethernet	Intel 82562GZ, IEEE 802.3u 10/100Base-T compatible Built-in boot ROM in Flash BIOS Optional PCI Express Intel 82573L IEEE 802.3u 1000Base-T compatible
CRT Display mode	Pixel resolution up to 1600 x 1200 at 85 Hz and 2048 x 1536 at 75 Hz
LCD Display mode	Dual channel LVDS panel supports up to UXGA panel resolution with frequency range from 25 MHz to 112 MHz
Dimensions (L x W)	95 x 125 (3.74" x 4.92")
Power Supply Voltage	+12 V power only
Power Requirement	Max: +12 V @ 4 A
Operating Temperature	0 ~ 60°C (32 ~ 140°F)
Operating Humidity	0% ~ 90% relative humidity, non-condensing

2.2.3 SOM-DB5700

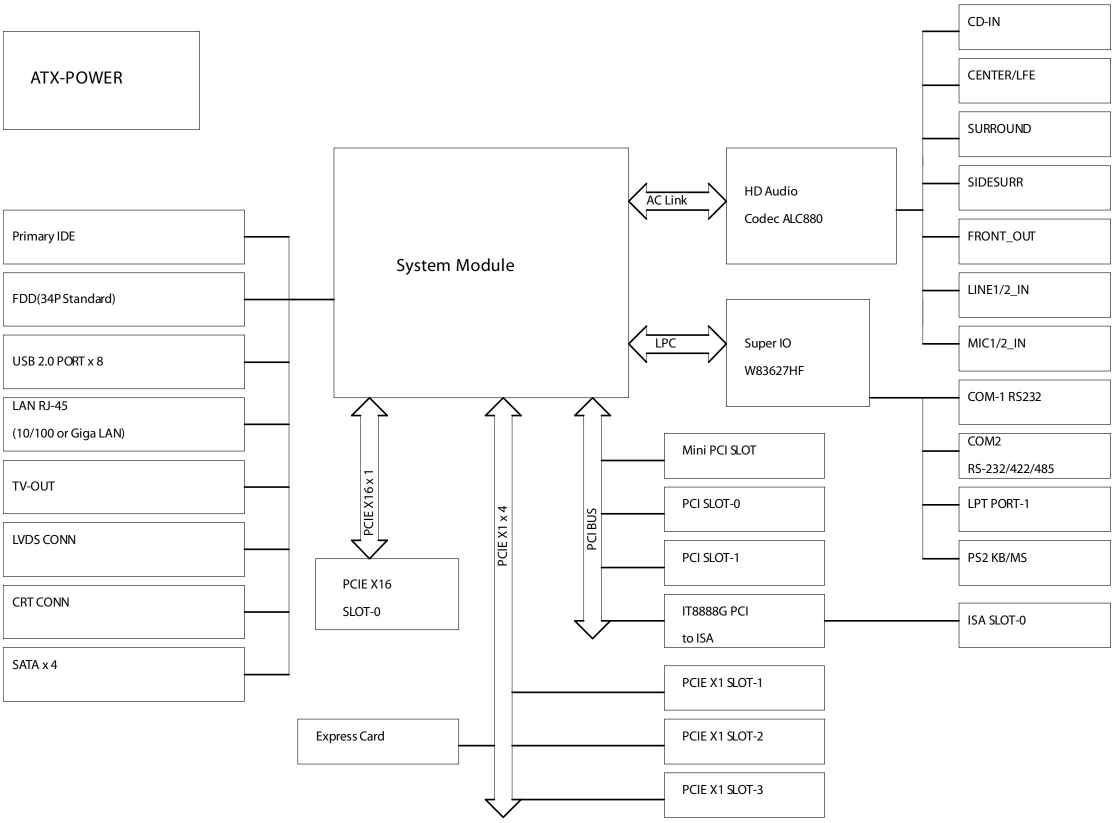


Figure 2-3 SOM-DB5700 Block Diagram

SOM-DB5700 Main Features:

Offers standard PC environment
PCI Express / PCI /ISA expansion interface
Reference design and prototype platform
ATX form factor

Table 2.3 SOM-DB5700 Specifications	
Item	**Description**
Extended	Four PCI Express bus and Three PCI bus and One ISA
Display	DB-15 VGA connector, LCD connector
Communications	DB-9 COM1 connector, 10-pin COM2 box header, RJ-45 Ethernet connector
MIO	EIDE/FDD/LPT/Keyboard/Mouse /USB/Audio/TV-out/SSD interface
Size/Weight	304.8 x 190.5 mm (12" x 7.5"), 0.37 kg (0.81 lb)

2.3 System Resources

This section demonstrates resources distribution of Advantech's SOM-Express modules, including IRQ, DMA, memory map, and I/O map.

2.3.1 SOM-5780 Resources

Table 2.4 SOM-5780 IRQ Resources

IRQ	Description
0	(ISA) System timer
1	(ISA) Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
2	-
3	(ISA) Communications Port (COM2)
4	(ISA) Communications Port (COM1)
5	-
6	(ISA)Standard floppy disk controller
7	(ISA)ECP Printer Port (LPT1)
8	(ISA) System CMOS/real time clock
9	(ISA) Microsoft ACPI-Compliant System, Intel(R) 82801FBM SMBus Controller - 24C3
10	-
11	-
12	(ISA) PS/2 Compatible Mouse
13	(ISA) Numeric data processor
14	(ISA) Primary IDE Channel
15	(ISA) Secondary IDE Channel
16	(PCI) Intel(R) 82915 GM Graphics Controller, Intel(R) 82801FBM USB Universal Host Controller - 24C2
17	(PCI) Realtek AC'97 Audio
18	(PCI) Intel(R) 82801FBM USB Universal Host Controller - 24C7
19	(PCI) 19 Intel(R) 82801FBM USB Universal Host Controller - 24C4
20	-
21	-
22	-
23	(PCI) Intel PCI to USB Enhanced Host Controller

Table 2.5 SOM-5780 DMA Resources

DMA	Description
0	Cascade to DMA4
1	-
2	Standard floppy disk controller
3	ECP Printer Port (LPT1)
4	Direct memory access controller
5	-
6	-
7	-

Table 2.6 SOM-5780 Memory Map	
Memory Address	**Description**
00000000 - 0009FFFF	System board
000A0000 - 000BFFFF	PCI bus
000A0000 - 000BFFFF	Intel(R) 82915GM Graphics Controller
000C0000 - 000DFFFF	PCI bus
000E0000 - 000EFFFF	System board
000F0000 - 000F3FFF	System board
000F4000 - 000F7FFF	System board
000F8000 - 000FBFFF	System board
000FC000 - 000FFFFF	System board
00100000 - 0DFEFFFF	System board
0DFF0000 - 0DFFFFFF	System board
0E000000 - FEBFFFFF	PCI bus
D8000000 - DFFFFFFF	Intel(R) 82915GM Graphics Controller
E0000000 - E7FFFFFF	Intel(R) 82915GM Graphics Controller
E8000000 - E807FFFF	Intel(R) 82915GM Graphics Controller
E8080000 - E80FFFFF	Intel(R) 82915GM Graphics Controller
E8100000 - E81003FF	Intel PCI to USB Enhanced Host Controller
E8101000 - E81011FF	Realtek AC'97 Audio
E8102000 - E81020FF	Realtek AC'97 Audio
FEBFFC00 - FEBFFFFF	Intel(R) 82801FBM Ultra ATA Storage Controller - 24CB
FEC00000 - FECFFFFF	System board
FEE00000 - FEEFFFFF	System board
FFB00000 - FFB7FFFF	System board
FFB80000 - FFBFFFFF	Intel(r) 82802 Firmware Hub Device
FFF00000 - FFFFFFFF	System board

Table 2.7 SOM-5780 I/O Map

Memory Address	Description
00000000 - 00000CF7	PCI bus
00000000 - 0000000F	Direct memory access controller
00000010 - 0000001F	Motherboard resources
00000020 - 00000021	Programmable interrupt controller
00000022 - 0000003F	Motherboard resources
00000040 - 00000043	System timer
00000044 - 0000005F	Motherboard resources
00000060 - 00000060	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
00000061 - 00000061	System speaker
00000062 - 00000063	Motherboard resources
00000064 - 00000064	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
00000065 - 0000006F	Motherboard resources
00000070 - 00000073	System CMOS/real time clock
00000074 - 0000007F	Motherboard resources
00000080 - 00000090	Direct memory access controller
00000091 - 00000093	Motherboard resources
00000094 - 0000009F	Direct memory access controller
000000A0 - 000000A1	Programmable interrupt controller
000000A2 - 000000BF	Motherboard resources
000000C0 - 000000DF	Direct memory access controller
000000E0 - 000000EF	Motherboard resources
000000F0 - 000000FF	Numeric data processor
00000170 - 00000177	Secondary IDE Channel
000001F0 - 000001F7	Primary IDE Channel
00000274 - 00000277	ISAPNP Read Data Port
00000279 - 00000279	ISAPNP Read Data Port
000002F8 - 000002FF	Communications Port (COM2)
00000376 - 00000376	Secondary IDE Channel
00000378 - 0000037F	Printer Port (LPT1)
000003B0 - 000003BB	Intel(R) 82915GM Graphics Controller
000003C0 - 000003DF	Intel(R) 82915GM Graphics Controller
000003F6 - 000003F6	Primary IDE Channel
000003F8 - 000003FF	Communications Port (COM1)
00000400 - 000004BF	Motherboard resources
000004D0 - 000004D1	Motherboard resources
00000500 - 0000051F	Intel(R) 82801FBM SMBus Controller - 24C3
00000778 - 0000077B	Printer Port (LPT1)
00000A78 - 00000A7B	Motherboard resources
00000B78 - 00000B7B	Motherboard resources
00000BBC - 00000BBF	Motherboard resources
00000D00 - 0000FFFF	PCI bus
00000E78 - 00000E7B	Motherboard resources
00000F78 - 00000F7B	Motherboard resources
00000FBC - 00000FBF	Motherboard resources
0000E000 - 0000E007	Intel(R) 82915GM Graphics Controller
0000E100 - 0000E11F	Intel(R) 82801FBM USB Universal Host Controller - 24C2
0000E200 - 0000E21F	Intel(R) 82801FBM USB Universal Host Controller - 24C4
0000E300 - 0000E31F	Intel(R) 82801FBM USB Universal Host Controller - 24C7
0000E500 - 0000E5FF	Realtek AC'97 Audio
0000E600 - 0000E63F	Realtek AC'97 Audio
0000F000 - 0000F00F	Intel(R) 82801FBM Ultra ATA Storage Controller - 24CB

Table 2.8 SOM-5780 Alternative Device Resources	
Alternative Device Resources	
COM1	3F8/IRQ4*, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3, Disable
COM2	3F8/IRQ4, 2F8/IRQ3*, 3E8/IRQ4, 2E8/IRQ3, Disable
LPT1	378/IRQ7*, 278/IRQ5, 3BC/IRQ7, Disable

* Default setting

2.3.2 SOM-5782 Resources

Table 2.9 SOM-5782 IRQ Resources

IRQ	Description
0	(ISA) System timer
1	(ISA) Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
2	-
3	(ISA) Communications Port (COM2)
4	(ISA) Communications Port (COM1)
5	-
6	(ISA) Standard floppy disk controller
7	(ISA) ECP Printer Port (LPT1)
8	(ISA) System CMOS/real time clock
9	(ISA) Microsoft ACPI-Compliant System
10	-
11	(PCI) Intel(R) 82801G(ICH7 Family) SMBus Controller - 27DA
12	(ISA) PS/2 Compatible Mouse
13	(ISA) Numeric data processor
14	(ISA) Primary IDE Channel
15	(ISA) Secondary IDE Channel
16	(PCI) Intel(R) 82801G(ICH7 Family) PCI Express Root Port - 27D0
16	(PCI) Intel(R) 82801G(ICH7 Family) USB Universal Host Controller – 27CB
16	(PCI) Mobile Intel(R) 945GM Express Chipset Family
17	(PCI) Intel(R) PRO/1000 PL Network Connection
18	(PCI) Intel(R) 82801G(ICH7 Family) USB Universal Host Controller – 27CA
19	(PCI) Intel(R) 82801G(ICH7 Family) PCI Express Root Port - 27D6
19	(PCI) Intel(R) 82801G(ICH7 Family) USB Universal Host Controller – 27C9
19	(PCI) Intel(R) 82801GR/GH/GHM (ICH7 Family) PCI Express Root Port – 27E2
23	(PCI) Intel(R) 82801G(ICH7 Family) USB Universal Host Controller – 27CB
23	(PCI) Intel(R) 82801G(ICH7 Family) USB2 Enhanced Host Controller – 27CC

Table 2.10 SOM-5782 DMA Resources

DMA	Description
0	-
1	-
2	Standard floppy disk controller
3	-
4	Direct memory access controller
5	-
6	-
7	-

Table 2.11 SOM-5782 Memory Map

Memory Address	Description
0x0000-0x9FFFF	System board
0x100000-0xF6DFFFF	System board
0xA0000-0xBFFFF	PCI bus
0xA0000-0xBFFFF	Mobile Intel(R) 945GM Express Chipset Family
0xC0000-0xDFFFF	PCI bus
0xCE600-0xCFFFF	System board
0xD0000000-0xDFFFFFFF	Mobile Intel(R) 945GM Express Chipset Family
0xE0000-0xEFFFF	System board
0xE0000000-0xEFFFFFFF	Motherboard resources
0xF0000-0xF7FFF	System board
0xF6E0000-0xF6FFFFF	System board
0xF700000-0xFEBFFFFF	PCI bus
0xF8000-0xFBFFF	System board
0xFC000-0xFFFFF	System board
0xFD600000-0xFD6FFFFF	Intel(R) 82801G (ICH7 Family) PCI Express Root Port - 27D0
0xFD900000-0xFD9FFFFF	Intel(R) 82801G (ICH7 Family) PCI Express Root Port - 27D0
0xFDA00000-0xFDAFFFFF	Intel(R) 82801GR/GH/GHM (ICH7 Family) PCI Express Root Port - 27E2
0xFDB00000-0xFDCFFFFF	Intel(R) 82801GR/GH/GHM (ICH7 Family) PCI Express Root Port - 27E2
0xFDB00000-0xFDCFFFFF	Intel(R) PRO/1000 PL Network Connection
0xFDCE0000-0xFDCFFFFF	Intel(R) PRO/1000 PL Network Connection
0xFDD00000-0xFDDFFFFF	Intel(R) 82801G (ICH7 Family) PCI Express Root Port - 27D6
0xFDE00000-0xFDEFFFFF	Intel(R) 82801G (ICH7 Family) PCI Express Root Port - 27D6
0xFDF00000-0xFDF7FFFF	Mobile Intel(R) 945GM Express Chipset Family
0xFDF80000-0xFDFBFFFF	Mobile Intel(R) 945GM Express Chipset Family
0xFDFF8000-0xFDFFBFFF	PCI Device
0xFDFFF000-0xFDFFF3FF	Intel(R) 82801G (ICH7 Family) USB2 Enhanced Host Controller - 27CC
0xFEC00000-0xFEC00FFF	System board
0xFED13000-0xFED1DFFF	System board
0xFED20000-0xFED8FFFF	System board
0xFEE00000-0xFEE00FFF	System board
0xFFB00000-0xFFB7FFFF	System board
0xFFB80000-0xFFBFFFFF	Intel(r) 82802 Firmware Hub Device
0xFFF00000-0xFFFFFFFF	System board

Table 2.12 SOM-5782 I/O Map	
Memory Address	Description
0x0000-0x0CF7	PCI bus
0x0000-0x0CF7	Direct memory access controller
0x0010-0x001F	Motherboard resources
0x0020-0x0021	Programmable interrupt controller
0x0022-0x003F	Motherboard resources
0x0040-0x0043	System timer
0x0044-0x005F	Motherboard resources
0x0060-0x0060	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
0x0061-0x0061	System speaker
0x0062-0x0063	Motherboard resources
0x0064-0x0064	Standard 101/102-Key or Microsoft Natural PS/2 Keyboard
0x0065-0x006F	Motherboard resources
0x0070-0x0073	System CMOS/real time clock
0x0074-0x007F	Motherboard resources
0x0080-0x0090	Direct memory access controller
0x0091-0x0093	Motherboard resources
0x0094-0x009F	Direct memory access controller
0x00A0-0x00A1	Programmable interrupt controller
0x00A2-0x00BF	Motherboard resources
0x00C0-0x00DF	Direct memory access controller
0x00E0-0x00EF	Motherboard resources
0x00F0-0x00FF	Numeric data processor
0x0170-0x0177	Secondary IDE Channel
0x01F0-0x01F7	Primary IDE Channel
0x0274-0x0277	ISAPNP Read Data Port
0x0279-0x0279	ISAPNP Read Data Port
0x02F8-0x02FF	Communications Port (COM2)
0x0376-0x0376	Secondary IDE Channel
0x0378-0x037F	Printer Port (LPT1)
0x03B0-0x03BB	Mobile Intel(R) 945GM Express Chipset Family
0x03C0-0x03DF	Mobile Intel(R) 945GM Express Chipset Family
0x03F0-0x03F5	Standard floppy disk controller
0x03F6-0x03F6	Primary IDE Channel
0x03F7-0x03F7	Standard floppy disk controller
0x03F8-0x03FF	Communications Port (COM1)
0x0400-0x04BF	Motherboard resources
0x04D0-0x04D1	Motherboard resources
0x0500-0x051F	Intel(R) 82801G (ICH7 Family) SMBus Controller - 27DA
0x0680-0x06FF	Motherboard resources
0x0778-0x077B	Printer Port (LPT1)
0x0880-0x088F	Motherboard resources
0x0A78-0x0A7B	Motherboard resources
0x0B78-0x0B7B	Motherboard resources
0x0BBC-0x0BBF	Motherboard resources
0x0D00-0xFFFF	PCI bus
0x0E78-0x0E7B	Motherboard resources
0x0F78-0x0F7B	Motherboard resources
0x0FBC-0x0FBF	Motherboard resources
0xA000-0xAFFF	Intel(R) 82801G (ICH7 Family) PCI Express Root Port - 27D0
0xB000-0xBFFF	Intel(R) 82801GR/GH/GHM (ICH7 Family) PCI Express Root Port - 27E2
0xBF00-0xBF1F	Intel(R) PRO/1000 PL Network Connection
0xC000-0xCFFF	Intel(R) 82801G (ICH7 Family) PCI Express Root Port - 27D6

0xEA00-0xEA0F	Intel(R) 82801GBM/GHM (ICH7-M Family) Serial ATA Storage Controller - 27C4
0xEB00-0xEB1F	Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27CB
0xEC00-0xEC1F	Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27CA
0xED00-0xED1F	Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27C9
0xEE00-0xEE1F	Intel(R) 82801G (ICH7 Family) USB Universal Host Controller - 27C8
0xEF00-0xEF07	Mobile Intel(R) 945GM Express Chipset Family

Table 2.13 SOM-5782 Alternative Device Resources

Alternative Device Resources	
COM1	3F8/IRQ4*, 2F8/IRQ3, 3E8/IRQ4, 2E8/IRQ3, Disable
COM2	3F8/IRQ4, 2F8/IRQ3*, 3E8/IRQ4, 2E8/IRQ3, Disable
LPT1	378/IRQ7*, 278/IRQ5, 3BC/IRQ7, Disable

2.4 PCI Routing

Table 2.14 Advantech SOM-Express Module PCI Routing

SOM-5780	PCI Device	IRQ	REQ	GNT	IDSEL
	82541PI	INTB#	REQ5	GNT5	AD25
	-	-	-	-	-

2.5 DC Specifications

The Advantech's SOM-Express modules power consumption properties have been measured and list in Table 6.1

2.5.1 Interface I/O Voltage

2.5.1.1 PCI Bus

Table 2.15 DC specifications for 5V signaling of PCI Bus

Symbol	**Parameter**	**Min**	**Max**	**Units**	**Note**
Vcc	Supply Voltage	4.75	5.25	V	
Vih	Input High Voltage	2.0	Vcc+0.5	V	
Vil	Input Low Voltage	-0.5	0.8	V	
Voh	Output High Voltage	2.4	-	V	
Vol	Output Low Voltage	-	0.55	V	*1

*1. Signals without pull-up resistors must have 3 mA low output current. Signals requiring pull up must have 6 mA; the latter include, FRAME#, TRDY#, IRDY#, DEVSEL#, STOP#, SERR#, PERR#, LOCK#, INTA#, INTB#, INTC#, INTD#.

Table 2.16 DC specifications for 3.3V signaling of PCI Bus					
Symbol	**Parameter**	**Min**	**Max**	**Units**	**Note**
Vcc	Supply Voltage	3.0	3.6	V	
Vih	Input High Voltage	0.5Vcc	Vcc+0.5	V	
Vil	Input Low Voltage	-0.5	0.3Vcc	V	
Vipu	Input Pull-up Voltage	0.7Vcc	-	V	*1
Voh	Output High Voltage	0.9Vcc	-	V	
Vol	Output Low Voltage	-	0.1Vcc	V	

*1. This specification should be guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Applications sensitive to static power utilization must assure that the input buffer is conducting minimum current at this input voltage.

2.5.1.2 Universal Serial Bus (USB)

Table 2.17 DC specification of USB signals					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Note**
V_{bus}	High-power port supply voltage	4.75	5.25	V	
V_{bus}	Low-power port supply voltage	4.75	5.25	V	
V_{IL}	Input Low Voltage	-	0.8	V	
V_{IH}	Input High Voltage(driven)	2.0	-	V	
V_{IHZ}	Input High Voltage(floating)	2.7	3.6	V	
V_{OL}	Output Low Voltage	0	0.3	V	
V_{OH}	Output High Voltage	2.8	3.6	V	

2.5.1.3 Audio

Table 2.18 AC'97 CODEC DC specification					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Note**
Dvdd	Digital supply voltage	Dvdd+5%	Dvdd+5%	V	
Avdd	Analog supply voltage	4.75	5.25	V	
Vil	Input Low Voltage	-	0.35Vdd	V	
Vih	Input High Voltage	0.65Vdd	-	V	

*1. Dvdd=5V or 3.3V

Table 2.19 AC'97 CODEC analog I/O DC specification						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Unit**	**Note**
AUXAL/R	Full scale input voltage	-	1.0	-	Vrms	
MIC	Full scale input voltage	-	0.1	-	Vrms	
SNDL/R	Full scale output voltage	-	1.0	-	Vrms	

2.5.1.4 VGA

Table 2.20 Hsync and Vsync signals specification					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Note**
V_{IL}	Input Low Voltage	0	0.5	V	
V_{IH}	Input High Voltage	2.4	5.5	V	
V_{OL}	Output Low Voltage	-	0.8	V	
V_{OH}	Output High Voltage	2.0	-	V	

Table 2.21 RGB Voltage					
Symbol	**Parameter**	**Min**	**Max**	**Unit**	**Note**
R	Red analog video output signal Max. luminance voltage	0.665	0.77	V	
G	Green analog video output signal Max. luminance voltage	0.665	0.77	V	
B	Blue analog video output signal Max. luminance voltage	0.665	0.77	V	
R	Red analog video output signal min. luminance voltage	0 (Typical)		V	
G	Green analog video output signal min. luminance voltage	0 (Typical)		V	
B	Blue analog video output signal min. luminance voltage	0 (Typical)		V	

2.5.1.5 LCD

Table 2.22 LCD I/O Voltage

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	Vcc+0.5	V	
V_{OL}	Output Low Voltage	-	0.55	V	Iol=4.0mA
V_{OH}	Output High Voltage	2.4	-	V	Ioh=-1.0mA

2.5.1.6 IDE

Table 2.23 Ultra DMA modes 1-4 (5V)

Symbol	Parameter	Min	Max	Unit	Note
V_{IH}	Input High Voltage	-	5.5	V	
V_{OL}	Output Low Voltage	-	0	V	
V_{OH}	Output High Voltage	2	-	V	

Table 2.24 Ultra DMA modes 5 (3.3V)

Symbol	Parameter	Min	Max	Unit	Note
V_{dd3}	DC supply voltage to drivers and receivers	3.3-8%	3.3+8%	V	
V+	Low to High input threshold	1.5	2.0	V	
V_-	High to Low input threshold	1.0	1.5	V	

2.5.1.7 Ethernet

Table 2.25 Ethernet I/O Voltage

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Input Low Voltage	-0.5	0.3Vcc	V	*1
V_{IH}	Input High Voltage	0.5Vcc	Vcc+0.5	V	
V_{OL}	Ouput Low Voltage	-	0.1Vcc		
V_{OH}	Output High Voltage	0.9Vcc	Vcc		

*1. Vcc=3.0V min. to 3.6V max.

2.5.1.8 TV-Out Bus

Table 2.26 TV-Out I/O Voltage

Symbol	Parameter	Min	Max	Unit	Note
V_O	Output Voltage	1.28	1.28	V	Typical=1.8
V_{IH}	Input High Voltage	0	1.4	V	

2.5.1.9 IrDA

Table 2.27 IrDA I/O Voltage

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	VCC+0.5	V	
V_{OL}	Output Low Voltage	-	0.4	V	
Voh	Output High Voltage	2.4	-	V	
I_{Ldtx}	Input Load Current (IRTX Signal)	-	6	mA	$0 \leqq Vin \leqq Vcc$
ILd	Input Load Current (all signal except IRTX)	-	1.5	mA	$0 \leqq Vin \leqq Vcc$

*1. From ”Infrared Data Association – Infrared Dongle Interface v1.1”
*2. Vcc=5.0V±5%

2.5.1.10 I2C

Table 2.28 I2C I/O Voltage

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Input Low Voltage	-0.5	0.3Vdd	V	
V_{IH}	Input High Voltage	0.7Vdd	Vdd+0.5	V	
V_{OL}	Output Low Voltage	0	0.4	V	

*1. The I2C Bus Specification V2.1.
*2. Vdd is the voltage which the pull-up resistor are connected.

2.5.1.11 SMBus

Table 2.29 SMBus I/O Voltage

Symbol	Parameter	Min	Max	Unit	Note
V_{IL}	Input Low Voltage	-	0.8	V	
V_{IH}	Input High Voltage	2.1	Vdd	V	
V_{OL}	Output Low Voltage	-	0.4	V	

*1. System Management Bus (SMBus) Specification v2.0.
*2. Vdd is the voltage which the pull-up resistor are connected.

2.6 AC Specification

2.6.1 PCI-Bus AC Spec.

Refer to “PCI Local Bus Specification Revision 2.2 December 18, 1998” Chapter 4.2 for the details.

2.6.2 Universal Serial Bus (USB) AC Spec.

Refer to “Universal Serial Bus Specification Revision 1.1 September 23, 1998” Chapter 7 for the details.

2.6.3 Audio AC Spec.

Refer to “Audio Codec ’97 Revision 2.1 May 22, 1998” Chapter 9 for digital signals AC spec. and Chapter 10 for analog performance spec.

2.6.4 VGA AC Spec.

Please refer to “VESA and Industry Standards and Guidelines for Computer Display Monitor Timing Version 1.0, Revision 0.8” for the monitor timing specification.

2.6.5 IDE AC Spec.

Please refer to “Information Technology - AT Attachment with Packet Interface – 7 Volume 2
(ATA/ATAPI-7 V2)” Annex B.5 for the details

2.6.6 I2C AC Spec.

Please refer to “THE I 2C-BUS SPECIFICATION VERSION 2.1 JANUARY 2000” for the DAC AC Characteristics

2.6.7 SMBus AC Spec.

Please refer to “System Management Bus (SMBus) Specification Version 2.0 August 3, 2000”

Chapter 3 Pin Assignments

This chapter describes pin assignments and IO characteristics for the 440 pin SOM-Express. It includes four parts (A, B, C, D). There are five types of pin assignments for COM-Express. We chose **type-2 pin assignments** on the SOM-Express. Please refer to the COM-Express specifications to get more information.

Figure 3-1 SOM-Express Diagram

Table 3.1 Conventions and Terminology		
Convention	**Description**	**Example**
'#'	Active-Low Signals	WAKE0#
'+' and '-'	Differential Pairs	SATA0_TX+, SATA0_TX-
Terminology	**Description**	
Pin Types:		
I	Input	
O	Output	
IO	Bi-Directional	
OD	Open Drain	
Power Pin Types		
VCC2.5	+2.5 V ± 5% Volts	
VCC3	+3.3 V ± 5% Volts	
VSB3	+3.3 V ± 5% Standby Power	
VCC3/5	+3.3 V and +5 V tolerance	
GND	System Ground	
PWR	Power Supply	
AC on	AC coupled on module	
AC off	AC coupled off module	
Others		
I/F	Interface	
MISC	Miscellaneous Interface	
NC	Not Connected. Reserved.	
P	Power Plane	
RSVD	Reserved pin	
*1	GND min, 3.3 V max	
REF	Reference voltage output. May be sourced from a module power plane.	
PDS	Pull-down strap. A module output pin that is either tied to GND or is not connected. Used to signal module capabilities to the Carrier Board.	

Notes:

1. PWR*: The power to this pin is supplied from the **carrier board** connected to the power supply.
2. Please refer to Chapter 5 for detailed descriptions.

3.1 Row A

Table 3.2 Connector A Pin Assignments

Pin	Signal	I/F	I/O	P	Pin	Signal	I/F	I/O	P
A1	GND (FIXED)	PWR	PWR*	-	**A56**	PCIE_TX4-	PCIE	O	AC on
A2	GBE0_MDI3-	GBE	IO	VSB3	**A57**	GND	PWR	PWR*	-
A3	GBE0_MDI3+	GBE	IO	VSB3	**A58**	PCIE_TX3+	PCIE	O	AC on
A4	GBE0_LINK100#	GBE	OD	VSB3	**A59**	PCIE_TX3-	PCIE	O	AC on
A5	GBE0_LINK1000#	GBE	OD	VSB3	**A60**	GND (FIXED)	PWR	PWR*	-
A6	GBE0_MDI2-	GBE	IO	VSB3	**A61**	PCIE_TX2+	PCIE	O	AC on
A7	GBE0_MDI2+	GBE	IO	VSB3	**A62**	PCIE_TX2-	PCIE	O	AC on
A8	GBE0_LINK#	GBE	OD	VSB3	**A63**	GPI1	MISC	I	VCC3
A9	GBE0_MDI1-	GBE	IO	VSB3	**A64**	PCIE_TX1+	PCIE	O	AC on
A10	GBE0_MDI1+	GBE	IO	VSB3	**A65**	PCIE_TX1-	PCIE	O	AC on
A11	GND (FIXED)	PWR	PWR*	-	**A66**	GND	PWR	PWR*	-
A12	GBE0_MDI0-	GBE	IO	VSB3	**A67**	GPI2	MISC	I	VCC3
A13	GBE0_MDI0+	GBE	IO	VSB3	**A68**	PCIE_TX0+	PCIE	O	AC on
A14	GBE0_CTREF	GBE	REF	*1	**A69**	PCIE_TX0-	PCIE	O	AC on
A15	SUS_S3#	PSM	O	VSB3	**A70**	GND(FIXED)	PWR	PWR*	-
A16	SATA0_TX+	SATA	O	AC on	**A71**	LVDS_A0+	LVDS	O	-
A17	SATA0_TX-	SATA	O	AC on	**A72**	LVDS_A0-	LVDS	O	-
A18	SUS_S4#	PSM	O	VSB3	**A73**	LVDS_A1+	LVDS	O	-
A19	SATA0_RX+	SATA	I	AC on	**A74**	LVDS_A1-	LVDS	O	-
A20	SATA0_RX-	SATA	I	AC on	**A75**	LVDS_A2+	LVDS	O	-
A21	GND (FIXED)	PWR	PWR*	-	**A76**	LVDS_A2-	LVDS	O	-
A22	SATA2_TX+	SATA	O	AC on	**A77**	LVDS_VDD_EN	LVDS	O	VCC3
A23	SATA2_TX-	SATA	O	AC on	**A78**	LVDS_A3+	LVDS	O	-
A24	SUS_S5#	PSM	O	VSB3	**A79**	LVDS_A3-	LVDS	O	-
A25	SATA2_RX+	SATA	I	AC on	**A80**	GND(FIXED)	PWR	PWR*	
A26	SATA2_RX-	SATA	I	AC on	**A81**	LVDS_A_CK+	LVDS	O	-
A27	BATLOW#	PSM	I	VSB3	**A82**	LVDS_A_CK-	LVDS	O	-
A28	ATA_ACT#	SATA	O	VCC3	**A83**	LVDS_I2C_CK	LVDS	O	VCC3
A29	AC_SYNC	Audio	O	VCC3	**A84**	LVDS_I2C_DAT	LVDS	IO OD	VCC3
A30	AC_RST#	Audio	O	VSB3	**A85**	GPI3	MISC	I	VCC3
A31	GND (FIXED)	PWR	PWR*	-	**A86**	KBD_RST#	MISC	I	VCC3
A32	AC_BITCLK	Audio	IO	VCC3	**A87**	KBD_A20GATE	MISC	I	VCC3
A33	AC_SDOUT	Audio	O	VCC3	**A88**	PCIE0_CK_REF+	PCIE	O	VCC3
A34	BIOS_DISABLE#	MISC	I	VCC3	**A89**	PCIE0_CK_REF-	PCIE	O	VCC3
A35	THRMTRIP#	PSM	O	VSB3	**A90**	GND (FIXED)	PWR	PWR*	
A36	USB6-	USB	IO	VSB3	**A91**	RSVD	RSVD	-	-
A37	USB6+	USB	IO	VSB3	**A92**	RSVD	RSVD	-	-
A38	USB_6_7_OC#	USB	I	VSB3	**A93**	GPO0	MISC	O	VCC3
A39	USB4-	USB	IO	VSB3	**A94**	RSVD	RSVD	-	-
A40	USB4+	USB	IO	VSB3	**A95**	RSVD	RSVD	-	-
A41	GND (FIXED)	PWR	PWR*	-	**A96**	GND	PWR	PWR*	-
A42	USB2-	USB	IO	VSB3	**A97**	VCC_12V	PWR	PWR*	-
A43	USB2+	USB	IO	VSB3	**A98**	VCC_12V	PWR	PWR*	-
A44	USB_2_3_OC#	USB	I	VSB3	**A99**	VCC_12V	PWR	PWR*	-
A45	USB0-	USB	IO	VSB3	**A100**	GND (FIXED)	PWR	PWR*	-
A46	USB0+	USB	IO	VSB3	**A101**	VCC_12V	PWR	PWR*	-
A47	VCC_RTC	PWR	PWR*	-	**A102**	VCC_12V	PWR	PWR*	-
A48	EXCD0_PERST#	EXCD	O	VCC3	**A103**	VCC_12V	PWR	PWR*	-
A49	EXCD0_CPPE#	EXCD	I	VCC3	**A104**	VCC_12V	PWR	PWR*	-
A50	LPC_SERIRQ	LPC	IO	VCC3	**A105**	VCC_12V	PWR	PWR*	-
A51	GND(FIXED)	PWR	PWR*	-	**A106**	VCC_12V	PWR	PWR*	-
A52	PCIE_TX5+	PCIE	O	AC on	**A107**	VCC_12V	PWR	PWR*	-
A53	PCIE_TX5-	PCIE	O	AC on	**A108**	VCC_12V	PWR	PWR*	-
A54	GPI0	MISC	I	VCC3	**A109**	VCC_12V	PWR	PWR*	-
A55	PCIE_TX4+	PCIE	O	AC on	**A110**	GND (FIXED)	PWR	PWR*	-

3.2 Row B

Table 3.3 Connector B Pin Assignments

Pin	Signal	I/F	I/O	P	Pin	Signal	I/F	I/O	P
B1	GND (FIXED)	PWR	PWR*	-	B56	PCIE_RX4-	PCIE	I	AC off
B2	GBE0_ACT#	GBE	OD	VSB3	B57	GPO2	MISC	O	VCC3
B3	LPC_FRAME#	LPC	O	VCC3	B58	PCIE_RX3+	PCIE	I	AC off
B4	LPC_AD0	LPC	IO	VCC3	B59	PCIE_RX3-	PCIE	I	AC off
B5	LPC_AD1	LPC	IO	VCC3	B60	GND (FIXED)	PWR	PWR*	-
B6	LPC_AD2	LPC	IO	VCC3	B61	PCIE_RX2+	PCIE	I	AC off
B7	LPC_AD3	LPC	IO	VCC3	B62	PCIE_RX2-	PCIE	I	AC off
B8	LPC_DRQ0#	LPC	I	VCC3	B63	GPO3	MISC	O	VCC3
B9	LPC_DRQ1#	LPC	I	VCC3	B64	PCIE_RX1+	PCIE	I	AC off
B10	LPC_CLK	LPC	O	VCC3	B65	PCIE_RX1-	PCIE	I	AC off
B11	GND (FIXED)	PWR	PWR*	-	B66	WAKE0#	PSM	I	VSB3
B12	PWRBTN#	PSM	I	VSB3	B67	WAKE1#	PSM	I	VSB3
B13	SMB_CK	PSM	IO OD	VSB3	B68	PCIE_RX0+	PCIE	I	AC off
B14	SMB_DAT	PSM	IO OD	VSB3	B69	PCIE_RX0-	PCIE	I	AC off
B15	SMB_ALERT#	PSM	I	VSB3	B70	PWR	PWR*	-	PWR
B16	SATA1_TX+	SATA	O	AC on	B71	LVDS_B0+	LVDS	O	-
B17	SATA1_TX-	SATA	O	AC on	B72	LVDS_B0-	LVDS	O	-
B18	SUS_STAT#	PSM	O	VSB3	B73	LVDS_B1+	LVDS	O	-
B19	SATA1_RX+	SATA	I	AC on	B74	LVDS_B1-	LVDS	O	-
B20	SATA1_RX-	SATA	I	AC on	B75	LVDS_B2+	LVDS	O	-
B21	GND (FIXED)	PWR	PWR*	-	B76	LVDS_B2-	LVDS	O	-
B22	SATA3_TX+	SATA	O	AC on	B77	LVDS_B3+	LVDS	O	-
B23	SATA3_TX-	SATA	O	AC on	B78	LVDS_B3-	LVDS	O	-
B24	PWR_OK	PSM	I	VCC3	B79	LVDS_BKLT_EN	LVDS	O	VCC3
B25	SATA3_RX+	SATA	I	AC on	B80	GND(FIXED)	PWR	PWR*	
B26	SATA3_RX-	SATA	I	AC on	B81	LVDS_B_CK+	LVDS	O	-
B27	WDT	MISC	O	VCC3	B82	LVDS_B_CK-	LVDS	O	-
B28	AC_SDIN2	Audio	I	VSB3	B83	LVDS_BKLT_CTRL	LVDS	O	VCC3
B29	AC_SDIN1	Audio	I	VSB3	B84	VCC5V_SBY	PWR	PWR*	
B30	AC_SDIN0	Audio	I	VSB3	B85	VCC_5V_SBY	PWR	PWR*	
B31	GND (FIXED)	PWR	PWR*	-	B86	VCC_5V_SBY	PWR	PWR*	
B32	SPKR	MISC	O	VCC3	B87	VCC_5V_SBY	PWR	PWR*	
B33	I2C_CK	MISC	O	VCC3	B88	RSVD	RSVD	-	-
B34	I2C_DAT	MISC	IO OD	VCC3	B89	VGA_RED	VGA	O	-
B35	THRM#	PSM	I	VCC3	B90	GND (FIXED)	PWR	PWR*	-
B36	USB7-	USB	IO	VSB3	B91	VGA_GRN	VGA	O	-
B37	USB7+	USB	IO	VSB3	B92	VGA_BLU	VGA	O	-
B38	USB_4_5_OC#	USB	I	VSB3	B93	VGA_HSYNC	VGA	O	VCC3
B39	USB5-	USB	IO	VSB3	B94	VGA_VSYNC	VGA	O	VCC3
B40	USB5+	USB	IO	VSB3	B95	VGA_I2C_CK	VGA	O	VCC3
B41	GND (FIXED)	PWR	PWR*	-	B96	VGA_I2C_DAT	VGA	IO OD	VCC3
B42	USB3-	USB	IO	VSB3	B97	TV_DAC_A	TV OUT	O	-
B43	USB3+	USB	IO	VSB3	B98	TV_DAC_B	TV OUT	O	-
B44	USB_0_1_OC#	USB	I	VSB3	B99	TV_DAC_C	TV OUT	O	-
B45	USB1-	USB	IO	VSB3	B100	GND (FIXED)	PWR	PWR*	-
B46	USB1+	USB	IO	VSB3	B101	VCC_12V	PWR	PWR*	-
B47	EXCD1_PERST#	EXCD	O	VCC3	B102	VCC_12V	PWR	PWR*	-
B48	EXCD1_CPPE#	EXCD	I	VCC3	B103	VCC_12V	PWR	PWR*	-
B49	SYS_RESET#	PSM	I	VSB3	B104	VCC_12V	PWR	PWR*	-
B50	CB_RESET#	PSM	O	VSB3	B105	VCC_12V	PWR	PWR*	-
B51	GND(FIXED)	PWR	PWR*	-	B106	VCC_12V	PWR	PWR*	-
B52	PCIE_RX5+	PCIE	I	AC off	B107	VCC_12V	PWR	PWR*	-
B53	PCIE_RX5-	PCIE	I	AC off	B108	VCC_12V	PWR	PWR*	-
B54	GPO1	MISC	O	VCC3	B109	VCC_12V	PWR	PWR*	-
B55	PCIE_RX4+	PCIE	I	AC off	B110	GND (FIXED)	PWR	PWR*	-

3.3 Row C

Table 3.4 Connector C Pin Assignments

Pin	Signal	I/F	I/O	P	Pin	Signal	I/F	I/O	P
C1	GND (FIXED)	PWR	PWR*	-	C56	PEG_RX1-	PCIE	I	AC off
C2	IDE_D7	IDE	IO	VCC3/5	C57	TYPE1#	MISC	PDS	-
C3	IDE_D6	IDE	IO	VCC3/5	C58	PEG_RX2+	PCIE	I	AC off
C4	IDE_D3	IDE	IO	VCC3/5	C59	PEG_RX2-	PCIE	I	AC off
C5	IDE_D15	IDE	IO	VCC3/5	C60	GND (FIXED)	PWR	PWR*	
C6	IDE_D8	IDE	IO	VCC3/5	C61	PEG_RX3+	PCIE	I	AC off
C7	IDE_D9	IDE	IO	VCC3/5	C62	PEG_RX3-	PCIE	I	AC off
C8	IDE_D2	IDE	IO	VCC3/5	C63	RSVD	RSVD	-	-
C9	IDE_D13	IDE	IO	VCC3/5	C64	RSVD	RSVD	-	-
C10	IDE_D1	IDE	IO	VCC3/5	C65	PEG_RX4+	PCIE	I	AC off
C11	GND (FIXED)	PWR	PWR*	-	C66	PEG_RE4-	PCIE	I	AC off
C12	IDE_D14	IDE	IO	VCC3/5	C67	RSVD	RSVD	-	-
C13	IDE_IORDY	IDE	I	VCC3/5	C68	PEG_RX5+	PCIE	I	AC off
C14	IDE_IOR#	IDE	O	VCC3	C69	PEG_RX5-	PCIE	I	AC off
C15	PCI_PME#	PCI	I	VSB3/5	C70	GND(FIXED)	PWR	PWR*	
C16	PCI_GNT2#	PCI	O	VCC3/5	C71	PEG_RX6+	PCIE	I	AC off
C17	PCI_REQ2#	PCI	I	VCC3/5	C72	PEG_RX6-	PCIE	I	AC off
C18	PCI_GNT1#	PCI	O	VCC3/5	C73	SDVO_DATA	SDVO	IO OD	VCC2.5
C19	PCI_REQ1#	PCI	I	VCC3/5	C74	PEG_RX7+	PCIE	I	AC off
C20	PCI_GNT0#	PCI	O	VCC3/5	C75	PEG_RX7-	PCIE	I	AC off
C21	GND (FIXED)	PWR	PWR*	-	C76	GND	PWR	PWR*	-
C22	PCI_REQ0#	PCI	I	VCC3/5	C77	RSVD	RSVD	-	-
C23	PCI_RESET#	PCI	O	VSB3/5	C78	PEG_RX8+	PCIE	I	AC off
C24	PCI_AD0	PCI	IO	VCC3/5	C79	PEG_RX8-	PCIE	I	AC off
C25	PCI_AD2	PCI	IO	VCC3/5	C80	GND(FIXED)	PWR	PWR*	
C26	PCI_AD4	PCI	IO	VCC3/5	C81	PEG_RX9+	PCIE	I	AC off
C27	PCI_AD6	PCI	IO	VCC3/5	C82	PEG_RX9-	PCIE	I	AC off
C28	PCI_AD8	PCI	IO	VCC3/5	C83	RSVD	RSVD	-	-
C29	PCI_AD10	PCI	IO	VCC3/5	C84	GND	PWR	PWR*	-
C30	PCI_AD12	PCI	IO	VCC3/5	C85	PEG_RX10+	PCIE	I	AC off
C31	GND (FIXED)	PWR	PWR*	-	C86	PEG_RX10-	PCIE	I	AC off
C32	PCI_AD14	PCI	IO	VCC3/5	C87	GND	PWR	PWR*	-
C33	PCI_C/BE1#	PCI	IO	VCC3/5	C88	PEG_RX11+	PCIE	I	AC off
C34	PCI_PERR#	PCI	IO	VCC3/5	C89	PEG_RX11-	PCIE	I	AC off
C35	PCI_LOCK#	PCI	IO	VCC3/5	C90	GND (FIXED)	PWR	PWR*	
C36	PCI_DEVSEL#	PCI	IO	VCC3/5	C91	PEG_RX12+	PCIE	I	AC off
C37	PCI_IRDY#	PCI	IO	VCC3/5	C92	PEG_RX12-	PCIE	I	AC off
C38	PCI_C/BE2#	PCI	IO	VCC3/5	C93	GND	PWR	PWR*	-
C39	PCI_AD17	PCI	IO	VCC3/5	C94	PEG_RX13+	PCIE	I	AC off
C40	PCI_AD19	PCI	IO	VCC3/5	C95	PEG_RX13-	PCIE	I	AC off
C41	GND (FIXED)	PWR	PWR*	-	C96	GND	PWR	PWR*	-
C42	PCI_AD21	PCI	IO	VCC3/5	C97	RSVD	RSVD	-	-
C43	PCI_AD23	PCI	IO	VCC3/5	C98	PEG_RX14+	PCIE	I	AC off
C44	PCI_C/BE3#	PCI	IO	VCC3/5	C99	PEG_RX14-	PCIE	I	AC off
C45	PCI_AD25	PCI	IO	VCC3/5	C100	GND (FIXED)	PWR	PWR*	
C46	PCI_AD27	PCI	IO	VCC3/5	C101	PEG_RX15+	PCIE	I	AC off
C47	PCI_AD29	PCI	IO	VCC3/5	C102	PEG_RX15-	PCIE	I	AC off
C48	PCI_AD31	PCI	IO	VCC3/5	C103	GND	PWR	PWR*	-
C49	PCI_IRQA#	PCI	I	VCC3/5	C104	VCC_12V	PWR	PWR*	-
C50	PCI_IRQB#	PCI	I	VCC3/5	C105	VCC_12V	PWR	PWR*	-
C51	GND(FIXED)	PWR	PWR*	-	C106	VCC_12V	PWR	PWR*	-
C52	PEG_RX0+	PCIE	I	AC off	C107	VCC_12V	PWR	PWR*	-
C53	PEG_RX0-	PCIE	I	AC off	C108	VCC_12V	PWR	PWR*	-
C54	TYPE0#	MISC	PDS	-	C109	VCC_12V	PWR	PWR*	-
C55	PEG_RX1+	PCIE	I	AC off	C110	GND (FIXED)	PWR	PWR*	-

3.4 Row D

Table 3.5 Connector D Pin Assignments

Pin	Signal	I/F	I/O	P	Pin	Signal	I/F	I/O	P
D1	GND (FIXED)	PWR	PWR*	-	**D56**	PEG_TX1-	PCIE	O	
D2	IDE_D5	IDE	IO	VCC3/5	**D57**	TYPE2#	MISC	PDS	-
D3	IDE_D10	IDE	IO	VCC3/5	**D58**	PEG_TX2+	PCIE	O	AC on
D4	IDE_D11	IDE	IO	VCC3/5	**D59**	PEG_TX2-	PCIE	O	AC on
D5	IDE_D12	IDE	IO	VCC3/5	**D60**	GND (FIXED)	PWR	PWR*	-
D6	IDE_D4	IDE	IO	VCC3/5	**D61**	PEG_TX3+	PCIE	O	AC on
D7	IDE_D0	IDE	IO	VCC3/5	**D62**	PEG_TX3-	PCIE	O	AC on
D8	IDE_REQ	IDE	I	VCC3/5	**D63**	RSVD	RSVD	-	-
D9	IDE_IOW#	IDE	O	VCC3	**D64**	RSVD	RSVD	-	-
D10	IDE_ACK#	IDE	O	VCC3	**D65**	PEG_TX4+	PCIE	O	AC on
D11	GND (FIXED)	PWR	PWR*	-	**D66**	PEG_TX4-	PCIE	O	AC on
D12	IDE_IRQ	IDE	I	VCC3/5	**D67**	GND	PWR	PWR*	-
D13	IDE_A0	IDE	O	VCC3	**D68**	PEG_TX5+	PCIE	O	AC on
D14	IDE_A1	IDE	O	VCC3	**D69**	PEG_TX5-	PCIE	O	AC on
D15	IDE_A2	IDE	O	VCC3	**D70**	GND(FIXED)	PWR	PWR*	-
D16	IDE_CS1#	IDE	O	VCC3	**D71**	PEG_TX6+	PCIE	O	AC on
D17	IDE_CS3#	IDE	O	VCC3	**D72**	PEG_TX6-	PCIE	O	AC on
D18	IDE_RESET#	IDE	O	VCC3	**D73**	SDVO_CLK	SDVO	O	VCC2.5
D19	PCI_GNT3#	PCI	O	VCC3/5	**D74**	PEG_TX7+	PCIE	O	AC on
D20	PCI_REQ3#	PCI	I	VCC3/5	**D75**	PEG_TX7-	PCIE	O	AC on
D21	GND (FIXED)	PWR	PWR*	-	**D76**	GND	PWR	PWR*	-
D22	PCI_AD1	PCI	IO	VCC3/5	**D77**	IDE_CBLID#	IDE	I	VCC3/5
D23	PCI_AD3	PCI	IO	VCC3/5	**D78**	PEG_TX8+	PCIE	O	AC on
D24	PCI_AD5	PCI	IO	VCC3/5	**D79**	PEG_TX8-	PCIE	O	AC on
D25	PCI_AD7	PCI	IO	VCC3/5	**D80**	GND(FIXED)	PWR	PWR*	-
D26	PCI_C/BE0#	PCI	IO	VCC3/5	**D81**	PEG_TX9+	PCIE	O	AC on
D27	PCI_AD9	PCI	IO	VCC3/5	**D82**	PEG_TX9-	PCIE	O	AC on
D28	PCI_AD11	PCI	IO	VCC3/5	**D83**	RSVD	RSVD	-	-
D29	PCI_AD13	PCI	IO	VCC3/5	**D84**	GND	PWR	PWR*	-
D30	PCI_AD15	PCI	IO	VCC3/5	**D85**	PEG_TX10+	PCIE	O	AC on
D31	GND (FIXED)	PWR	PWR*	-	**D86**	PEG_TX10-	PCIE	O	AC on
D32	PCI_PAR	PCI	IO	VCC3/5	**D87**	GND	PWR	PWR*	-
D33	PCI_SERR#	PCI	IO OD	VCC3/5	**D88**	PEG_TX11+	PCIE	O	AC on
D34	PCI_STOP#	PCI	IO	VCC3/5	**D89**	PEG_TX11-	PCIE	O	AC on
D35	PCI_TRDY#	PCI	IO	VCC3/5	**D90**	GND (FIXED)	PWR	PWR*	-
D36	PCI_FRAME#	PCI	IO	VCC3/5	**D91**	PEG_TX12+	PCIE	O	AC on
D37	PCI_AD16	PCI	IO	VCC3/5	**D92**	PEG_TX12-	PCIE	O	AC on
D38	PCI_AD18	PCI	IO	VCC3/5	**D93**	GND	PWR	PWR*	-
D39	PCI_AD20	PCI	IO	VCC3/5	**D94**	PEG_TX13+	PCIE	O	AC on
D40	PCI_AD22	PCI	IO	VCC3/5	**D95**	PEG_TX13-	PCIE	O	AC on
D41	GND (FIXED)	PWR	PWR*	-	**D96**	GND	PWR	PWR*	-
D42	PCI_AD24	PCI	IO	VCC3/5	**D97**	PEG_ENABL#	PCIE	I	VCC3
D43	PCI_AD26	PCI	IO	VCC3/5	**D98**	PEG_TX14+	PCIE	O	AC on
D44	PCI_AD28	PCI	IO	VCC3/5	**D99**	PEG_TX14-	PCIE	O	AC on
D45	PCI_AD30	PCI	IO	VCC3/5	**D100**	GND (FIXED)	PWR	PWR*	-
D46	PCI_IRQC#	PCI	I	VCC3/5	**D101**	PEG_TX15+	PCIE	O	AC on
D47	PCI_IRQD#	PCI	I	VCC3/5	**D102**	PEG_TX15-	PCIE	O	AC on
D48	PCI_CLKRUN#	PCI	IO	VCC3/5	**D103**	GND	PWR	PWR*	-
D49	PCI_M66EN	PCI	I	VCC3/5	**D104**	VCC_12V	PWR	PWR*	-
D50	PCI_CLK	PCI	O	VCC3/5	**D105**	VCC_12V	PWR	PWR*	-
D51	GND(FIXED)	PWR	PWR*	-	**D106**	VCC_12V	PWR	PWR*	-
D52	PEG_TX0+	PCIE	O	AC on	**D107**	VCC_12V	PWR	PWR*	-
D53	PEG_TX0-	PCIE	O	AC on	**D108**	VCC_12V	PWR	PWR*	-
D54	PEG_LANE_RV#	PCIE	I	VCC3	**D109**	VCC_12V	PWR	PWR*	-
D55	PEG_TX1+	PCIE	O	AC on	**D110**	GND (FIXED)	PWR	PWR*	-

Chapter 4 General Design Recommendations

A brief description of the Printed Circuit Board (PCB) for SOM-Express based boards is provided in this section. From a cost- effectiveness point of view, a four-layer board is the target platform for the motherboard design. For better quality, a six-layer or 8-layer board is preferred.

4.1 Nominal Board Stack-Up

The trace impedance typically noted (55 Ω ± 10%) is the “nominal” trace impedance for a 5-mil wide external trace and a 4-mil wide internal trace. However, some stack-ups may lead to narrower or wider traces on internal or external layers in order to meet the 55-Ω impedance target, that is, the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. Note the trace impedance target assumes that the trace is not subjected to the EMI fields created by changing current in neighboring traces.

It is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces when calculating flight times. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. In order to minimize the effects of trace-to-trace coupling, the routing guidelines documented in this Section should be followed. Also, all high speed, impedance controlled signals should have continuous GND referenced planes and cannot be routed over or under power/GND plane splits.

4.1.1 Four layer board stack-up

Figure 4-1 illustrates an example of a four-layer stack-up with 2 signal layers and 2 power planes. The two power planes are the power layer and the ground layer. The layer sequence of component-ground-power-solder is the most common stack-up arrangement from top to bottom.

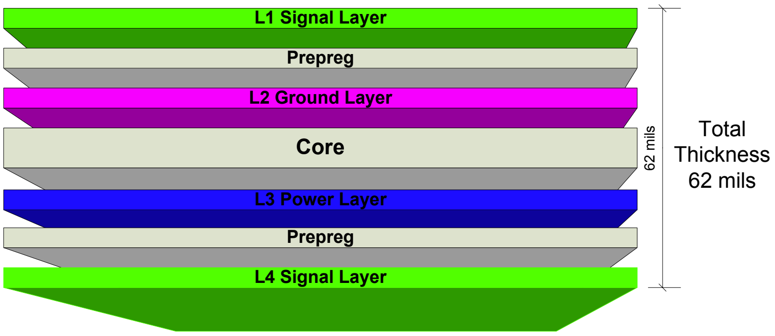


Figure 4-1 Four-Layer Stack-up

Table 4.1: Recommended Four-Layer Stack-Up Dimensions								
Dielectric Thickness (mil)	Layer	Layer	Signal-End Signals		Differential Signals		USB differential Signals	
	No	Type	Width (mil)	Impedance (ohm)	Width (mil)	Impedance (ohm)	Width (mil)	Impedance (ohm)
0.7	L1	Signals	6/6	55+/-10%	6/7/6	100+/-10%	6/5/6	90+/-10%
5		Prepreg						
1.4	L2	Ground						
47		Core						
1.4	L3	Power						
5		Prepreg						
0.7	L4	Signals	6/6	55+/-10%	6/7/6	100+/-10%	6/5/6	90+/-10%

Notes:
Target PCB Thickness totals 62mil+/-10%

4.1.2 Six layer board stack-up

Figure 4-2 illustrates an example of a six-layer stack-up with 4 signal layers and 2 power planes. The two power planes are the power layer and the ground layer. The layer sequence of component-ground-IN1-IN2-power-solder is the most common stack-up arrangement from top to bottom.

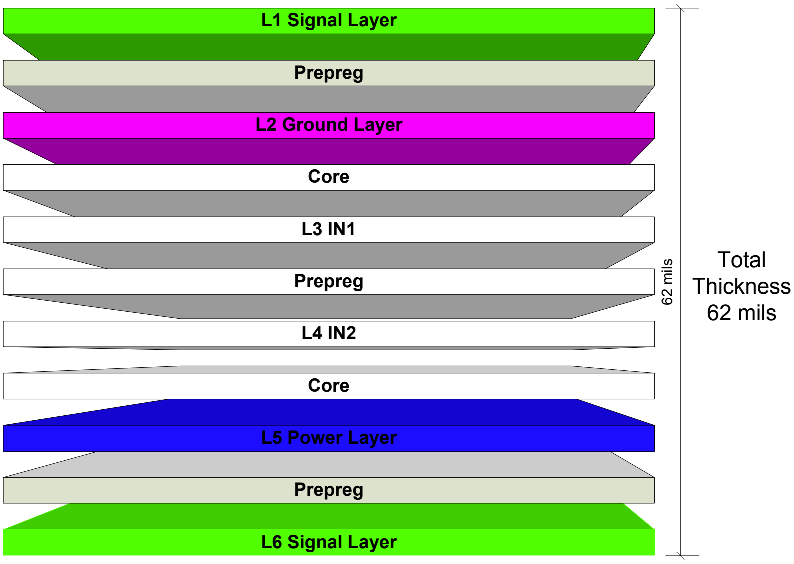


Figure 4-2 Six-Layer Stack-up

Table 4.2 Recommended Six-Layer Stack-Up Dimensions

Dielectric Thickness (mil)	Layer No	Layer Type	Single-End Signals		Differential Signals		USB differential Signals	
			Width (mil)	Impedance (ohm)	Width (mil)	Impedance (ohm)	Width (mil)	Impedance(ohm)
1.7	L1	Signals	5/5	55+/-10%	5/6/5	100+/-10%	5/4/5	90+/-10%
4		Prepreg						
1.4	L2	Ground						
5		Core						
1.4	L3	IN1	5/5	55+/-10%	4/8/4	100+/-10%	4/5/4	90+/-10%
35		Prepreg						
1.4	L4	IN2						
5		Core	5/5	55+/-10%	4/8/4	100+/-10%	4/5/4	90+/-10%
1.4	L5	Power						
4		Prepreg						
1.7	L6	Signals	5/5	55+/-10%	5/6/5	100+/-10%	5/4/5	90+/-10%

Notes:
Target PCB Thickness totals 62mil+/-10%

4.2 Differential Impedance Targets for Microstrip Routing

Table 4.3 shows the target impedance of the differential signals. The carrier board should follow the required impedance in this table.

Table 4.3 Differential Signals Impedance Requirement

Signal Type	Impedance
Host Clock	100 ohm +/- 20%
DMI	100 ohm +/- 20%
Ext Gfx-PCI Express Arch.	100 ohm +/- 20%
SDVO	100 ohm +/- 20%
LVDS	100 ohm +/- 20%
SATA	100 ohm +/- 20%
USB	90 ohm +/- 20%
PCI Express	100 ohm +/- 20%
DDR2 (clocks)	70 ohm +/- 20%
DDR2 (Strobes)	85 ohm +/- 20%
LAN	100 ohm +/- 20

4.3 Alternate Stack Ups

When customers choose to use different stack-ups (number of layers, thickness, trace width, etc.), the following key elements should be observed:

1. Final post lamination, post etching, and post plating dimensions should be used for electrical model extractions.
2. All high-speed signals should reference solid ground planes through the length of their routing and should not cross plane splits. To guarantee this, both planes surrounding strip-lines should be GND.
3. Recommends that high-speed signal routing be done on internal, strip-line layers. High-speed routing on external layers should be minimized in order to avoid EMI. Routing on external layers also introduces different delays compared to internal layers. This makes it extremely difficult to do length matching if routing is done on both internal and external layers.

Chapter 5 Carrier Board Design Guidelines

5.1 PCI-Bus

SOM-Express provides a PCI Bus interface that is compliant with the PCI Local Bus Specification, Revision 2.3. The implementation is optimized for high-performance data streaming when SOM-Express is acting as either the target or the initiator on the PCI bus. For more information on the PCI Bus interface, please refer to the PCI Local Bus Specification, Revision 2.3.

5.1.1 Signal Description

Table 5-1 shows SOM-Express PCI bus signal, including pin number, signals, I/0, and descriptions.

Table 5.1 PCI Signal Description

Pin	Signal	I/O	Description
D50	PCI_CLK	O	PCI 33 MHz clock output
D48	PCI_CLKRUN#	I/O	Bidirectional pin used to support PCI clock run protocol for mobile systems
C22,C19, C17,D20	PCI_REQ[0..3]	I	Bus Request signals for up to 4 external bus mastering PCI devices. When asserted, a PCI device is requesting PCI bus ownership from the arbiter.
C20,C18, C16,D19	PCI_GNT[0..3]	O	Grant signals to PCI Masters. When asserted by the arbiter, the PCI master has been granted ownership of the PCI bus.
-	PCI_AD[0..31]	I/O	PCI Address and Data Bus Lines. These lines carry the address and data information for PCI transactions.
D26,C33, C38,C44	PCI_C/BE[0..3]	I/O	PCI Bus Command and Byte Enables. Bus command and byte enables are multiplexed in these lines for address and data phases, respectively.
D32	PCI_PAR	I/O	Parity bit for the PCI bus.
D33	PCI_SERR#	I/O OD	System Error. Asserted for hardware error conditions such as parity errors detected in DRAM.
C34	PCI_PERR#	I/O	Parity Error. For PCI operation per exception granted by PCI 2.1 Specification.
C15	PME#	I	Power management event.
C35	PCI_LOCK#	I/O	Lock Resource Signal. This pin indicates that either the PCI master or the bridge intends to run exclusive transfers.
C36	PCI_DEVSEL#	I/O	Device Select, active low. When the target device has decoded the address as its own cycle, it will assert DEVSEL#.
D35	PCI_TRDY#	I/O	Target Ready. This pin indicates that the target is ready to complete the current data phase of a transaction.
C37	PCI_IRDY#	I/O	Initiator Ready. This signal indicates that the initiator is ready to complete the current data phase of a transaction.
D34	PCI_STOP#	I/O	Stop. This signal indicates that the target is requesting that the master stop the current transaction.
D36	PCI_FRAME#	I/O	Cycle Frame of PCI Buses. This indicates the beginning and duration of a PCI access.
C23	PCI_RESET#	I	PCI Bus Reset. This is an output signal to reset the entire PCI Bus. This signal is asserted during system reset.
C49,C50, D46,D47	PCI_IRQ[A…D]	I	PCI interrupt request lines.
D49	PCI_M66EN	I	Module input signal indicates whether an off-module PCI device is capable of 66 MHz operation. Pulled to GND by Carrier Board device or by Slot Card if the devices are NOT capable of 66 MHz operation. If the module is not capable of supporting 66 MHz PCI operation, this input may be a no-connect on the module. If the module is capable of supporting 66 MHz PCI operation, and if this input is held low by the Carrier Board, the module PCI interface shall operate at 33 MHz.

5.1.2 Design Guidelines

5.1.2.1 Differences among PCI Slots

Most PCI signals are connected in parallel to all the slots (or devices). The exceptions are the following pins from each slot or device:

Table 5.2 Carrier PCI Slots

IDSEL	: Connected (through resistor) to a different AD line for each slot.
CLK	: Connected to a different SOM-Express PCI clock signal for each slot.
INTA# ~ INTD#	: Connected to a different SOM-Express interrupt signal for each slot.
REQ#	: Connected to a different SOM-Express request signal for each slot, if used.
GNT#	: Connected to a different SOM-Express grant signal for each slot, if used.

Each signal connects differently for each of the four possible slots or devices as summarized in the following PCI Slots/Devices Table 5.3

Table 5.3 Carrier PCI Slots/Devices Interrupt Routing Table

SOM-EXPRESS	PCI Slot 0	PCI Slot 1	PCI Slot 2	PCI Slot 3
AD20 (Pin D39)	IDSEL	-	-	-
AD21 (Pin C42)	-	IDSEL	-	-
AD22 (Pin D40)	-	-	IDSEL	-
AD23 (Pin C43)	-	-	-	IDSEL
INTA# (Pin C49)	INTA#	INTB#	INTC#	INTD#
INTB# (Pin C50)	INTB#	INTC#	INTD#	INTA#
INTC# (Pin D46)	INTC#	INTD#	INTA#	INTB#
INTD# (Pin D47)	INTD#	INTA#	INTB#	INTC#

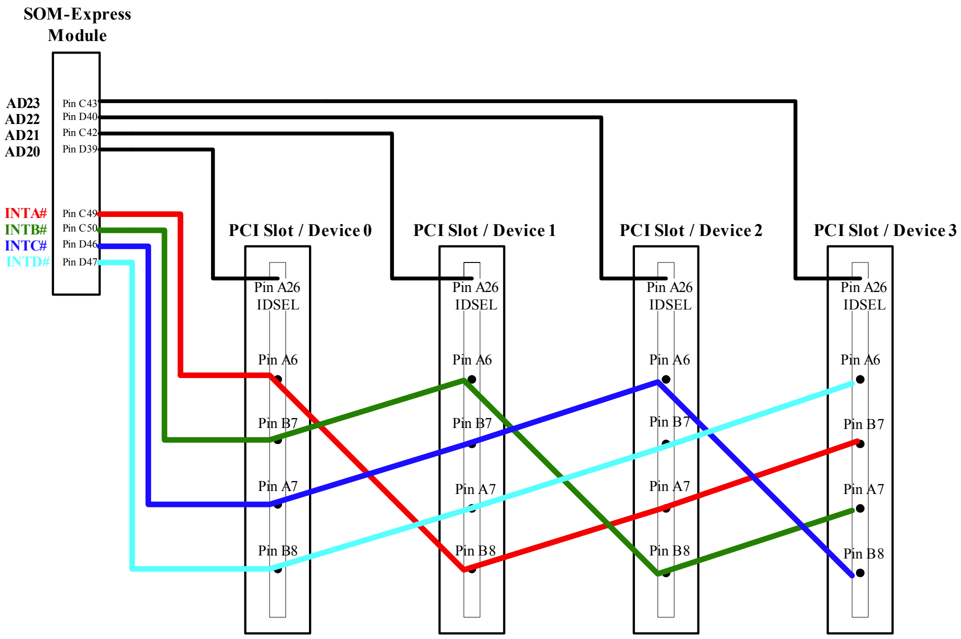


Figure 5-1 Routing PCI Slot/Device CSB Interrupt

Due to different system configurations, IRQ line routing to the PCI slots should be made to minimize the sharing of interrupts between both internal chipset functions and PCI functions. However, the INTA# pin of the device should not necessarily be connected to the SOM-Express INTA# signal. Please refer to 2.3.1 System Interrupt for more details.

5.1.2.2 PCI Clock and Clock Skew

The trace length for all PCI clocks should be matched and controlled. PCI clock routes should be separated as far from other signal traces as possible. PCI clock signals should be routed as controlled-impedance traces, with trace impedance of 55 Ω. Only one PCI device or slot should be driven from the SOM-Express PCI clock output.

The maximum allowable clock skew is 2 ns. This specification applies not only at a single threshold point, but at all points on the clock edge that fall in the switching range. The maximum skew is measured between any two components rather than between connectors. To correctly evaluate clock skew, the system designer must take into account clock distribution on the add-in card.

Table 5.4 Clock Skew Parameters

Symbol	3.3 V Signaling	5 V Signaling	Units
Vtest	0.4 Vcc	1.5	V
Tskew	2 (max)	2 (max)	ns

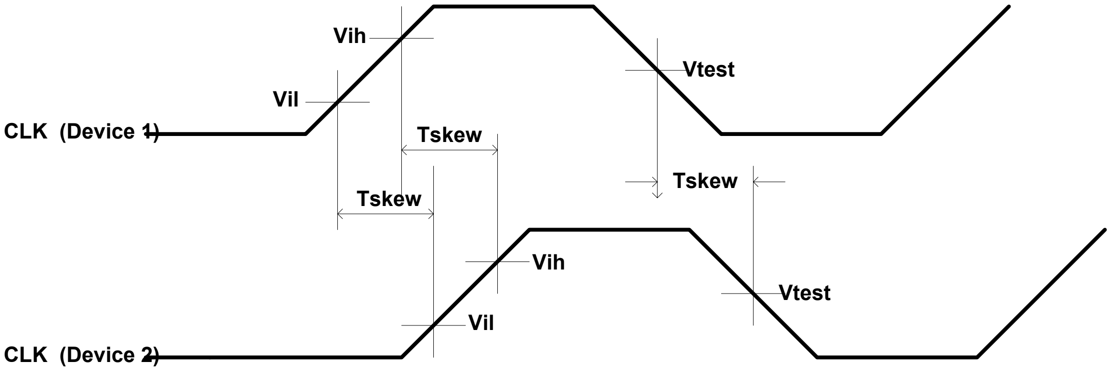


Figure 5-2 Clock Skew Diagram

5.1.2.3 Non-necessary Signals for Individual PCI device

A PCI device implemented directly on the carrier board uses a subset of the signals shown on the slot connector. Some pins on the slot connector are used for slot and PCI card management functions and are not necessary for the operation of the PCI device itself.

An individual PCI device will not have pins REQ64, ACK64, M66EN, PRSNT1, PRSNT2, SDONE, SBO#, or the reserved pins. Most devices do not implement the test pins TCK, TDO, TDI, TMS, and TRST. Most PCI devices use INTA# only and do not have a connection for INTB#, INTC# or INTD#.

5.1.2.4 Carrier Board PCI slot Power Requirements

All PCI connectors require four power rails: +5 V, +3.3 V, +12 V, and -12 V. Systems that provide PCI connectors are required to provide all four rails in every system with the current budget. Systems may optionally supply 3.3 Vaux power. Systems that do not support PCI bus power management must treat the 3.3 Vaux pin as reserved. There are no specific system requirements for current per connector on the 3.3 V and 5 V rails; this is system dependent. Note that an add-in card must limit its total power consumption to 25 watts (from all power rails). The system provides a total power budget for add-in cards that can be distributed between connectors in an arbitrary way. The PRSNTn# pins on the connector allow the system to optionally assess the power demand of each add-in card and determine if the installed configuration will run within the total power budget.

Table 5.5 Maximum Add-in Card Loading via Each Power Rail

Power Rail	**Add-in card**
3.3 V+/-0.3 V	7.6 A Max (System dependent)
5 V+/- 5 %	5 A Max (System dependent)
12 V+/- 5 %	500 mA Max.
-12 V +/- 5 %	100 mA Max.

5.1.2.5 SOM-Express PCI interface supply voltage

The SOM-Express PCI interface is a 3.3 V signaling environment but has 5 V tolerance for I/O signals. If a universal PCI connector is used at the carrier board, a jumper design to select Vio for 5 V and 3.3 V is necessary. Otherwise, the suitable Vio voltage should be designed for a 5 V or 3.3 V connector.

Table 5.6 Add-in Card Supplied Power Selection			
Symbol	3.3 V Connector	5 V Connector	Universal Connector
Vio	3.3 V	5 V	Jumper select

Note:

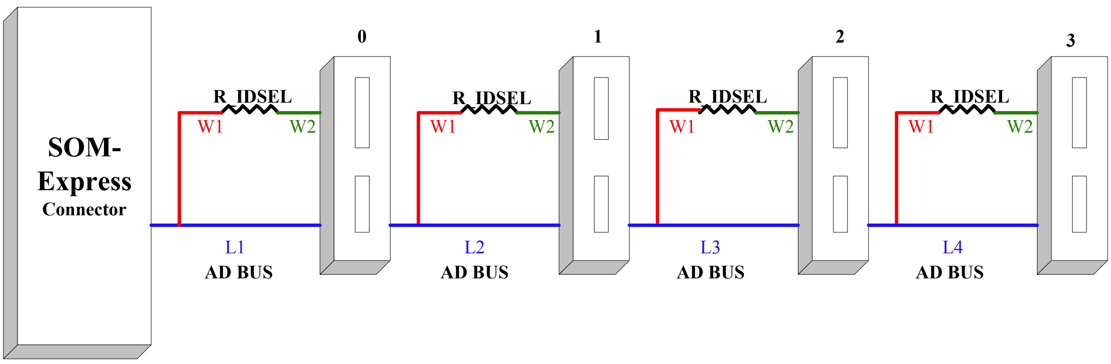
1. Note the riser card supply voltage and do not plug in the wrong supply voltage. If a universal connector is used, make sure the Vio jumper setting is correct when plugged into the riser card.
2. Advantech's demo carrier board provides a 5 V connector and 5 V Vio for PCI slots. Plugging a 3.3 V riser card in the wrong direction will cause carrier board or riser card damage.

5.1.3 Layout Guidelines

The following represents a summary of the routing guidelines for PCI devices. Simulations assume that PCI cards follow the PCI Local Bus Specification, Revision 2.3, trace length guidelines.

5.1.3.1 PCI Bus Layout Example with IDSEL

The following guidelines apply to platforms with nominal impedances of 55 Ω ± 10%.



PCI AD Bus should be routed as daisy chain to PCI expansion slots

Figure 5-3 PCI Bus Layout Example with IDSEL

Table 5.7 PCI Data Signals Routing Summary						
Trace Impedance	**PCI Routing Requirements**	**Topology**	**Maximum Trace Length (unit: inch)**			
			L1	L2	L3	L4
55 Ω +/- 10%	6 mils width, 6 mils spacing (based on stackup assumptions)	2 Slots W1 = W2 = 0.5 inches, R_IDSEL = 300 to 900.	10	1.0		
		3 Slots W1 = W2 = 0.5 inches, R_IDSEL = 300 to 900.	10	1.0	1.0	
		4 Slots W1 = W2 = 0.5 inches, R_IDSEL = 300 to 900.	10	1.1	1.1	1.1

5.1.3.2 PCI Clock Layout Example

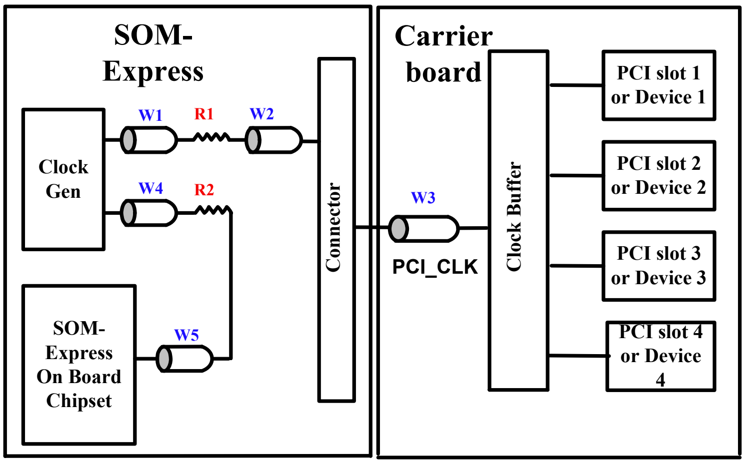


Figure 5-4 PCI Clock Layout Example

Table 5.8 PCI Clock Signals Routing Summary				
Trace Impedance	**PCI Routing Requirements**	**Topology**	**Maximum trace Length**	**Damping Resistor**
55 Ω +/- 10%	6 mils width, 50 mils spacing (based on stackup assumptions)	2 ~ 4 Devices	W1: 0.5 inch W2: 5 inches W3: 15 inches W4: 0.5 inch W5: as long as needed	R1: 33 Ω R2: 33 Ω

Note:
Clock skew between PCI slots/devices should be less than 2 ns@33 MHz and 1 ns@66 MHz. The recommended value of the clock trace tolerance of W3 (a,b,c,d) is 5 inches (Max).

5.1.4 Application Notes

5.1.4.1 REQ/GNT

These signals are used only by bus-mastering PCI devices. Most SOM-Express modules do not have enough REQ/GNT pairs available to support a bus-mastering device at every slot position. A PCI arbiter design is recommended when extra REQ/GNT pairs are required. Figure 5-5 shows an example design for PCI arbiter.

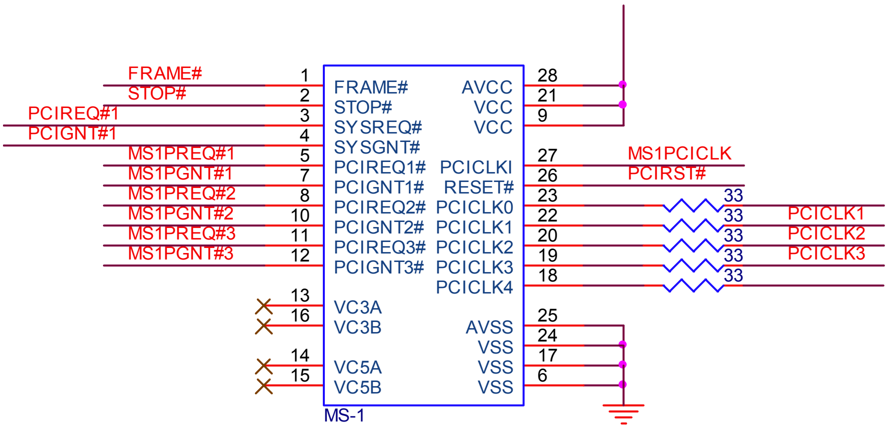


Figure 5-5 Design Example: PCI Arbiter

If there are less than four REQ/GNT pairs available for external devices, they will be assigned starting with the REQ0#/GNT0# pair. Therefore, external bus-mastering devices should be placed in the lowest numbered slot positions and non-bus mastering devices should be placed in the highest-numbered slot positions. Refer to Chapter 2.3.1 REQ/GNT for details.

5.1.4.2 PC104-Plus Connector

If a PC104-Plus connector is used, the same signals are attached to the connector but the pin numbers differ because of the different connector type. See the PC/104-Plus Specification Version 1.0, February 1997, PC/104 Consortium (www.pc104.org) for details.

5.2 Universal Serial Bus (USB)

The Universal Serial Bus (USB) provides a bi-directional, isochronous, hot-attachable Plug and Play serial interface for adding external peripheral devices such as game controllers, communication devices and input devices on a single bus. SOM-Express modules provide several USB 2.0 ports.

USB stands for Universal Serial Bus, an industry-standard specification for attaching peripherals to a computer. It delivers high performance, the ability to plug in and unplug devices while the computer is running, great expandability, and a wide variety of solutions.

5.2.1 Signal Description

Table 5.9 shows SOM-Express USB signals, including pin number, signals, I/0 and descriptions.

Table 5.9 USB Signals Description

Pin	Signal	I/O	Description
- -	USB[0:7]+ USB[0:7]-	I/O	USB differential pairs, channels 0 through 7
B44	USB_0_1_OC#	I	USB over-current sense, USB channels 0 and 1. A pull-up for this line **shall** be present on the module. An open drain driver from a USB current monitor on the Carrier Board **may** drive this line low.
A44	USB_2_3_OC#	I	USB over-current sense, USB channels 2 and 3. A pull-up for this line **shall** be present on the module. An open drain driver from a USB current monitor on the Carrier Board **may** drive this line low.
B38	USB_4_5_OC#	I	USB over-current sense, USB channels 4 and 5. A pull-up for this line **shall** be present on the module. An open drain driver from a USB current monitor on the Carrier Board **may** drive this line low.
A38	USB_6_7_OC#	I	USB over-current sense, USB channels 6 and 7. A pull-up for this line **shall** be present on the module. An open drain driver from a USB current monitor on the Carrier Board **may** drive this line low.

5.2.2 Design Guidelines

Figure 5-6 shows USB connections for SOM-Express USB signals.

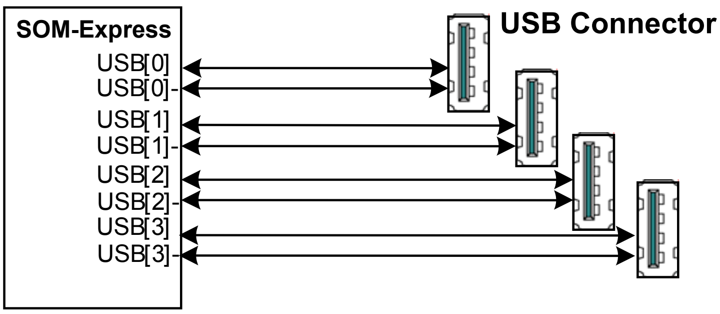


Figure 5-6 USB Connections

5.2.2.1 Low ESR Capacitor

You can hot plug USB devices. In fact, this is one of the virtues of USB relative to most other PC interfaces. The design of the USB power-decoupling network must absorb the momentary current surge from hot plugging an unpowered device. Reducing these values is not recommended. These capacitors should be low ESR, low inductance.

5.2.2.2 ESD or EMI suppression components

The following guidelines apply to the selection and placement of common mode chokes and ESD protection devices. Some USB designs will need additional ESD or EMI suppression components on the USB data lines. These are most effective when they are placed near the external USB connector and grounded to a low-impedance ground plane. SOM-Express modules vary in the number of USB ports that are implemented. Two ports are typical. Some SOM-Express modules implement three or four ports. If the application needs more than two USB ports, a low cost USB hub IC can be integrated onto the carrier board and connected to the USB0 or USB1 ports on the SOM-Express module. This provides a larger number of USB ports regardless of which SOM-Express module is in use.

A design may include a common mode choke footprint to provide a stuffing option in the event the choke is needed to pass EMI testing. Figure 5-7 shows the schematic of a typical common mode choke and ESD suppression components. The choke should be placed as close as possible to the USB connector signal pins.

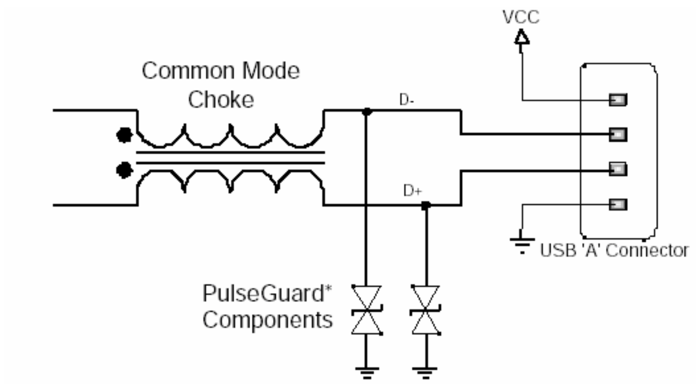


Figure 5-7 Common Mode Choke

Note:
ESD protection and common mode chokes are only needed if the design does not pass EMI or ESD testing. Basically, it is recommended to add them in the USB 2.0 interface. Footprints for common mode chokes and/or ESD suppression components should be included in the event that a problem occurs (General routing and placement guidelines should be followed).

5.2.3 Layout Guideline

5.2.3.1 Differential pairs

The USB data pairs (ex. USB [0] and USB [0]-) should be routed on the carrier board as differential pairs, with a differential impedance of 90 Ω. PCB layout software usually allows determining the correct trace width and spacing to achieve this impedance, after the PCB stack-up configuration is known.

As per usual differential pair routing practices, the two traces of each USB pair should be matched in length and kept at uniform spacing. Sharp corners should be avoided. At the SOM-Express module and connector ends of the routes, loop areas should be minimized. USB data pairs should be routed as far from other signals as possible.

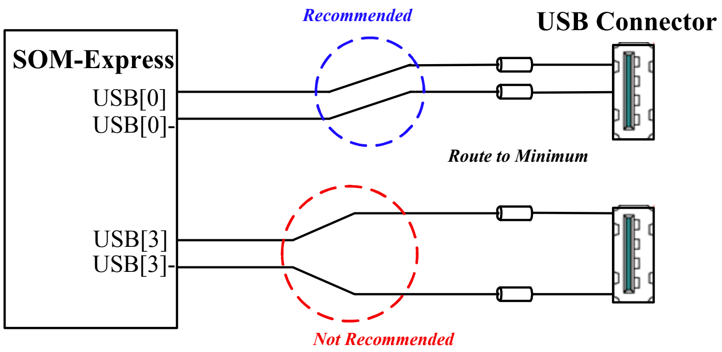


Figure 5-8 USB Layout Guidelines

5.2.3.2 Overcurrent Protection

Overcurrent protection on external USB power lines is required to prevent faults in external USB devices or cables from causing hardware damage and/or crashing the system. The USBOC# signal is used to signal overcurrent conditions to the system hardware and software. Note that overcurrent protection typically allows relatively high currents to flow for brief periods before the current is limited or interrupted. The system power supply must be able to provide these high currents while maintaining output regulation, or else the SOM-Express module or other system components may malfunction.

In case the simple resetable fuse (like shown on the reference schematic) does not switch off fast enough, overcurrent caused by an external USB device may impact the carrier boards internal power supply. In this case we recommend using active protection circuits available from various vendors. These devices may be used for per port protection of the USB power lines and allow direct connection to the USB_X_X_OC# signal.

NOTE: This circuit does not get implemented on SOM-Express. Please implement it on the carrier board.

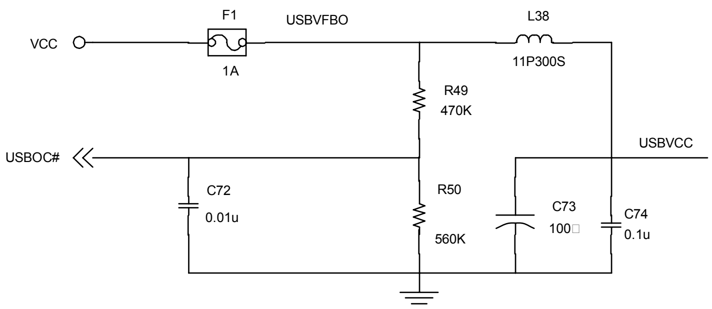


Figure 5-9 Overcurrent Circuit

5.2.3.3 Crossing a plane split

The mistake shown here is where the data lines cross a plane split. This causes unpredictable return path currents and would likely cause a signal quality failure as well as creating EMI problems.

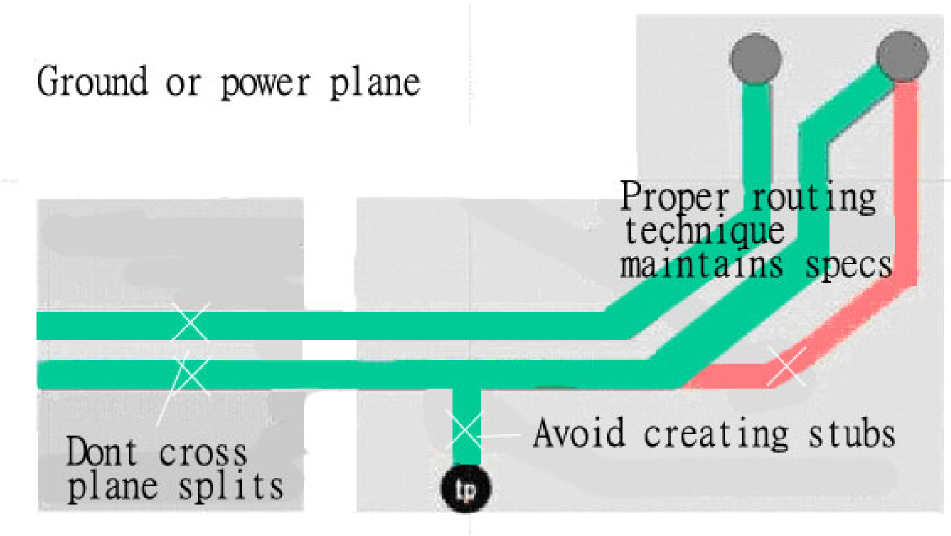


Figure 5-10 Violation of Proper Routing Techniques

5.2.3.4 Stubs

A very common routing mistake is shown in Figure 5-11. Here the designer could have avoided creating unnecessary stubs by proper placement of the pull down resistors over the path of the data traces. Once again, if a stub is unavoidable in the design, no stub should be greater than 200 mils. Here is another example where a stub is created that could have been avoided. Stubs typically cause degradation of signal quality and can also affect EMI.

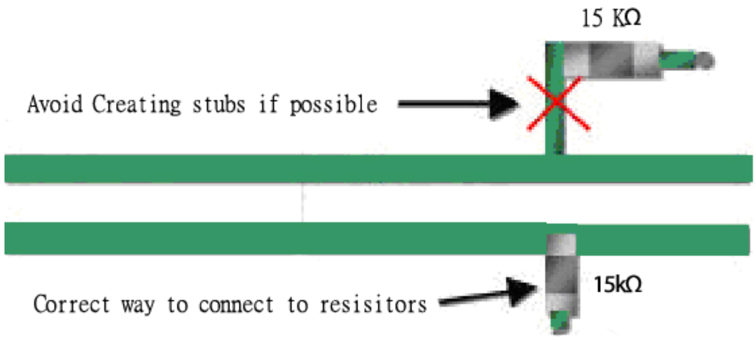


Figure 5-11 Creating Unnecessary Stubs

5.3 AC Link/Azalia interface

SOM-Express provides an AC Link/Azalia interface which is compliant to AC'97 Rev. 2.3 Specification and the Azalia Specification. Please establish the AC'97/Azalia CODEC on the carrier board for your application.

5.3.1 Signal Description

Table 5.10 shows SOM-Express AC Link/Azalia interface signals, including pin number, signals, I/0 and descriptions.

Table 5.10 Audio signals description

Pin	Signal	I/O	Description
A30	AC_RST#	O	**AC link / Azalia :** Reset output to AC97 CODEC, active low
A29	AC_SYNC	O	**AC link / Azalia :** 48 kHz fixed-rate, sample-synchronization signal to the CODEC(s)
A32	AC_BITCLK	I/O	**AC link:** Bit Clock Input: This signal is a 12.288 MHz serial data clock generated by the external codec(s). This signal has an integrated pull-down resistor **Azalia:** Bit Clock Output: This signal is a 24.000 MHz serial data clock generated by SOM-Express. This signal has an integrated pull-down resistor so that AC_BITCLK does not float when an Azalia codec (or no codec) is connected but the signals are temporarily configured as AC'97.
A33	AC_SDOUT	O	**AC link / Azalia :** Serial TDM data output to the CODEC
B30,B29, B28	AC_SDIN[0:2]	I	**AC link / Azalia :** Serial TDM data inputs from up to 3 CODECs

5.3.2 Design Guidelines

Azalia is the next generation architecture for implementing audio, modem, and communications functionality in the PC. The architecture of the SOM-Express Azalia-link allows a maximum of three CODECs to be connected.

5.3.2.1 Connection of AC link and Azalia

5.3.2.2 AC link:

Figure 5-12 shows the connections for SOM-Express AC link signals.
Clocking is provided from the primary codec on the link via AC_BITCLK, and is derived from a 24.576 MHz crystal or oscillator. Refer to the primary codec vendor for crystal or oscillator requirement. AC_BITCLK is a 12.288 MHz clock driven by the primary codec to the SOM-Express digital controller and to any other codec present.

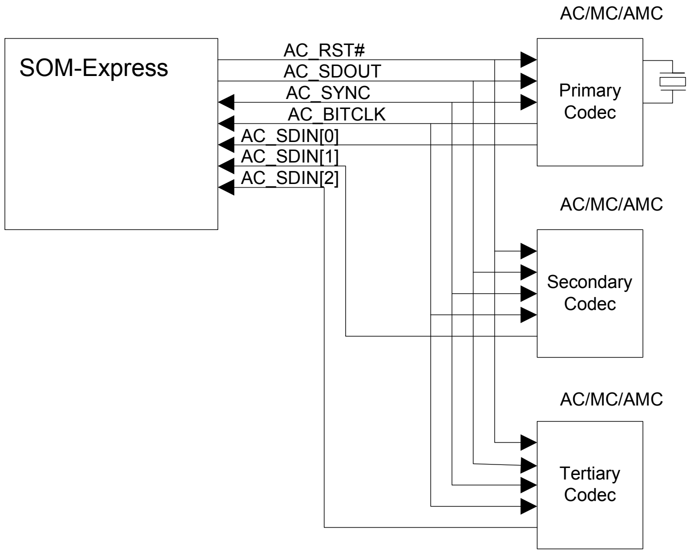


Figure 5-12 AC link Connections

5.3.2.3 Azalia:

Figure 5-13 shows the connections for SOM-Express Azalia signals. Azalia clocking is provided from SOM-Express via AC_BITCLK. AC_BITCLK is a 24.000 MHz clock driven by the SOM-Express to any codec present on the link

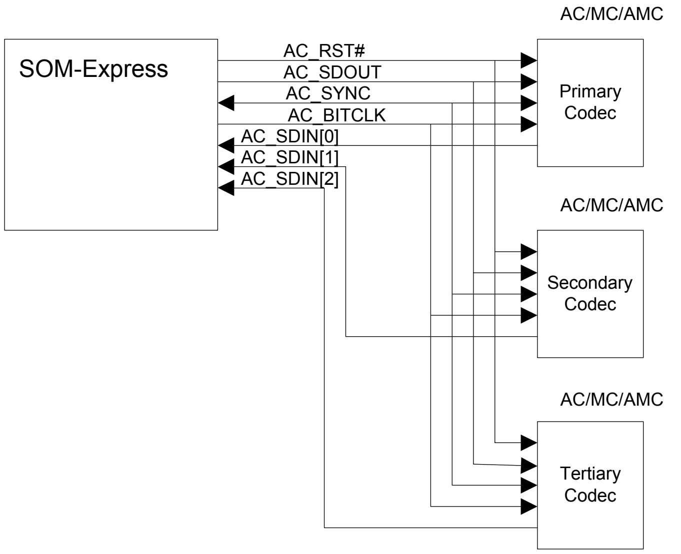


Figure 5-13 Azalia link Connections

Note: Azalia and AC'97 are mutually exclusive and cannot be used at the same time on a platform.

5.3.2.4 Codec Reference and Anti-Aliasing Recommendations

Place all ADC/DAC anti-aliasing filters and reference capacitors within 0.5 inches of their respective codec pins. All filter capacitors' ground connections should attach to ground trace from the codec to the capacitors without allowing vias to the digital ground plane. The audio codec should be placed in the quietest part (away from significant current paths and ground bounce) of the carrier board.

5.3.2.5 Grounding Techniques

Take care when grounding back panel audio jacks, especially the line in and microphone jacks. Avoid grounding the audio jacks to the ground plane directly under the connectors. Doing so raises the potential for audio noise to be induced on the inputs due to the difference in ground potential between the audio jacks and the codec's ground point. Figure 5-14 provides an AC' 97 example.

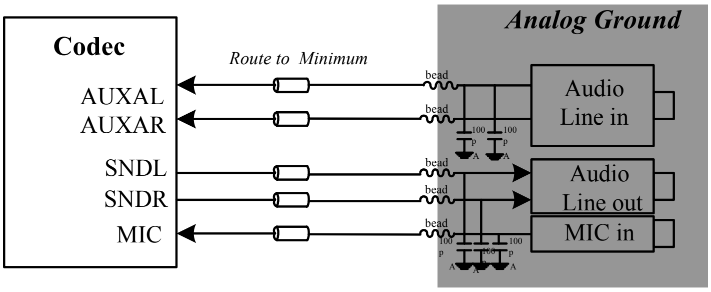


Figure 5-14 AC link Audio Layout Guidelines

5.3.2.6 AC link Stereo Microphone & Line In / Auxiliary In consideration

Back panel microphone input signal should be independent routed, and the ground return paths should be isolated from the carrier board ground plane. Use a capacitor to filter noise from the microphone bias net feeding all microphone jacks. Route microphone traces as far away as possible from non-microphone trace and digital traces. Audio designs that support up to 2 V RMS line input signals are recommended, but not required. To support audio inputs up to 2 V RMS, designs should implement a voltage divider network to effectively reduce the input level 6 dB prior to reaching the codec.

5.3.2.7 Azalia Audio Jack Consideration

The Azalia audio jack connectors should be designed to support up to two analog audio jacks, each of which can signal user connection to the operating system via sense resistor and a programmable GPIO signals. Figure 5-15 shows the example of sense resistor. Please see the codec specification to get more information.

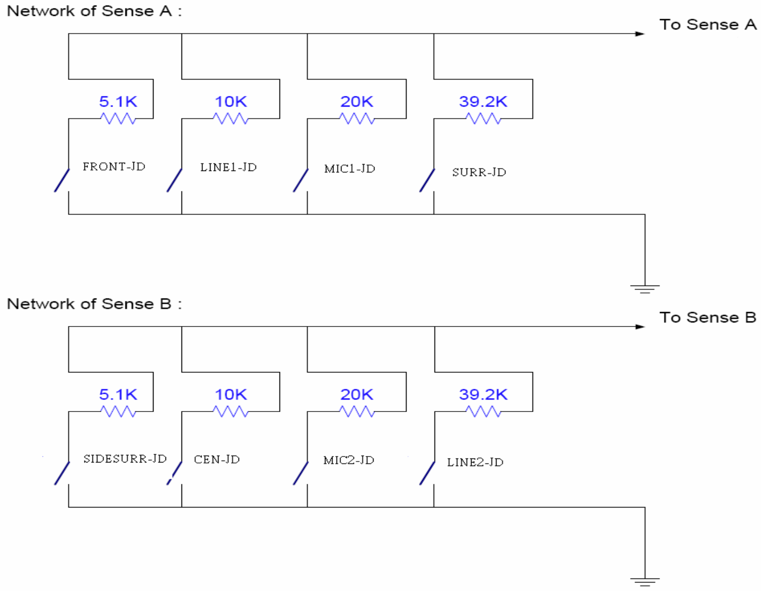


Figure 5-15 Sense resistor examples

5.3.3 Layout Guidelines

5.3.3.1 General Board Routing Recommendations

- Special consideration must be given for the ground return paths for the analog signals.
- Digital signals routed in the vicinity of the analog audio signals must not cross the power plane split. Located analog and digital signals as far as possible from each other.
- Partition the board with all analog components grouped together in one area and all digital components in another.
- Keep digital signal traces, especially the clock, as far away as possible from the analog input and voltage reference pins.
- All resistors in the signal path or on the voltage reference should be metal film. Carbon resistors can be used for DC voltages and the power supply path, where the voltage coefficient, temperature coefficient, and noise are not factors.
- Located the crystal or oscillation close to the codec.
- The AC link / Azalia trace impedance from codec to SOM-Express should be 55 Ω ± 15%.

5.3.3.2 EMI Consideration

Any signals entering or leaving the analog area must cross the ground split through bead in the area where the analog ground is attached to the main motherboard ground. That is, no signal should cross the split/gap between the ground planes, which would cause a ground loop, thereby greatly increasing EMI emissions and degrading the analog and digital signal quality.

5.3.3.3 Azalia Layout Guidelines

Figure 5-16 ~18 show the AC_SDIN, AC_SDOUT,AC_SYNC,AC_BITCLK,AC_RST# topology.
Table 5-11 ~ 13 show the routing summary.

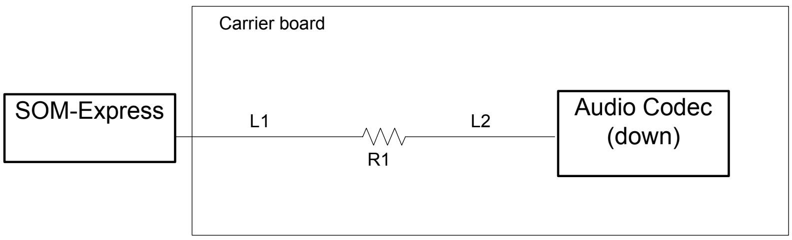


Figure 5-16 Azalia – AC_SDIN Topology

Table 5.11 Azalia – AC_SDIN Routing Summary				
Trace Impedance	**Azalia Requirements**	**Trace length**	**Series Termination Resistance**	**Signal Length Matching**
55 Ω +/- 15%	4 on 7 (stripline) 5 on 7 (microstrip)	L1= 1“ – 11“ L2= 0.5“	R1= 33 Ω	N/A

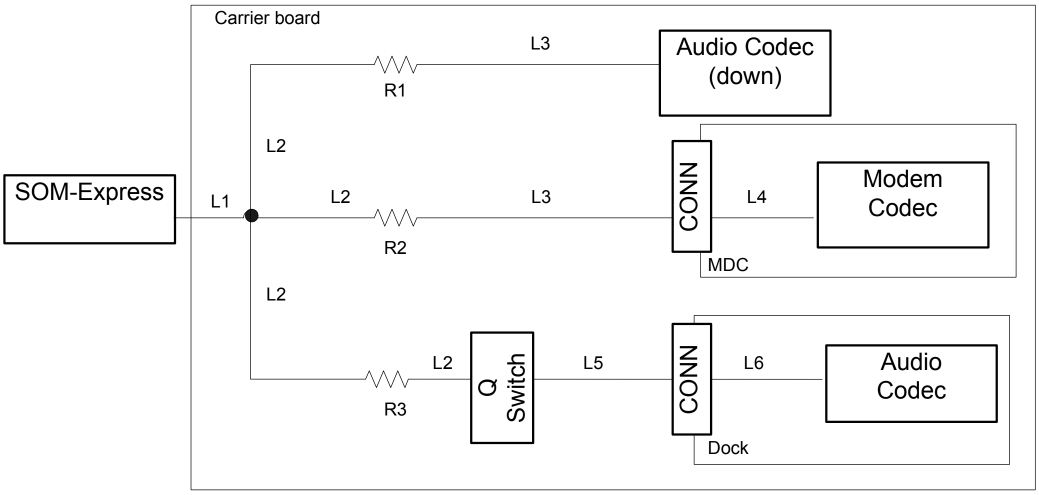


Figure 5-17 Azalia – AC_SDOUT/AC_SYNC/AC_BITCLK/AC_RST# Topology#1

Table 5.12 Azalia – AC_SDOUT/AC_SYNC/AC_ BITCLK/AC_RST# Topology #1				
Trace Impedance	**Azalia Requirements**	**Trace length**	**Series Termination Resistance**	**Signal Length Matching**
55 Ω +/- 15%	4 on 7 (stripline) 5 on 7 (microstrip)	L1= 1“ – 11“ L2= 0.5“ L3= 1“ – 15“ L4= 1.5“ L5≤0.5“ L6= 5“	R1= 33 Ω+/- 5% R2= 39 Ω+/- 5% R3= 39 Ω+/- 5%	N/A

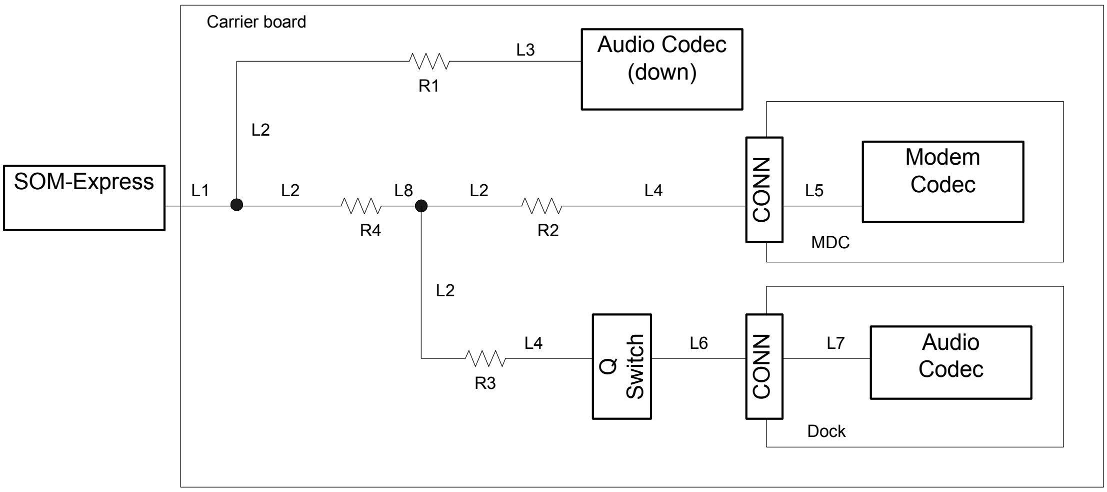


Figure 5-18 Azalia – AC_SDOUT/AC_SYNC/AC_BITCLK/AC_RST# Topology#2

Table 5.13 Azalia – AC_SDOUT/AC_SYNC/AC_ BITCLK/AC_RST# Topology #2				
Trace Impedance	**Azalia Requirements**	**Trace length**	**Series Termination Resistance**	**Signal Length Matching**
55 Ω +/- 15%	4 on 7 (stripline) 5 on 7 (microstrip)	L1= 0.5“ L2≤ 0.1“ L3= 1“ – 7“ L4= 1 - 5“ L5= 1.5“ L6≤ 0.5“ L7= 5“ L8= 0.1“ – 6“	R1= 39 Ω R2= 39 Ω R3= 39 Ω R4= 0 Ω	N/A

5.4 VGA

SOM-Express provides analog display signals. There are three signals -- red, green, and blue -- that send color information to a VGA monitor. These three signals each drive an electron gun that emits electrons which paint one primary color at a point on the monitor screen. Analog levels between 0 (completely dark) and 0.7 V (maximum brightness) on these control lines tell the monitor what intensities of these three primary colors to combine to make the color of a dot (or pixel) on the monitor's screen.

5.4.1 Signal Description

Table 5.14 shows SOM-Express VGA signals, including pin number, signals, I/0 and descriptions.

Table 5.14 VGA signals description			
Pin	**Signal**	**I/O**	**Description**
B89	VGA_RED	O	Red analog video output signal for CRT monitors, designed to drive a 37.5 Ω equivalent load.
B91	VGA_GRN	O	Green analog video output signals for CRT monitors, designed to drive a 37.5 Ω equivalent load.
B92	VGA_BLU	O	Blue analog video output signals for CRT monitors, designed to drive a 37.5 Ω equivalent load.
B93	VGA_HSYNC	O	Horizontal Sync: This output supplies the horizontal synchronization pulse to the CRT monitor.
B94	VGA_VSYNC	O	Vertical Sync: This output supplies the vertical synchronization pulse to the CRT monitor.
B95	VGA_I2C_CK	I/O	DDC clock line. It can be used for a DDC interface between the graphics controller chip and the CRT monitor
B96	VGA_I2C_DAT	I/O OD	DDC data line. It can be used for a DDC interface between the graphics controller chip and the CRT monitor

5.4.2 Design Guidelines

VESA standards require the DDC_PWR line. Some VGA monitors do not support the DDC standard. We suggest that VGA_I2C_CK and VGA_I2C_DAT signals must connect to the CRT monitor. They can be used for plug and play and monitor-type detection when standard monitors are attached.

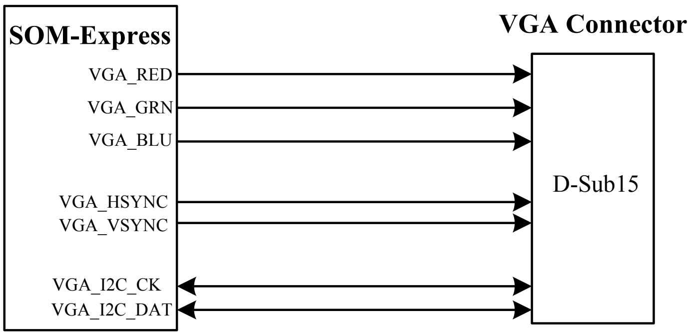


Figure 5-19 VGA Connections

5.4.3 Layout Guideline

5.4.3.1 RLC Components

The RGB outputs are current sources and therefore require 150 ohm load resistors from each RGB line to analog ground to create the output voltage (approximately 0 to 0.7 volts). These resistors should be placed near the VGA port (a 15-pin D-SUB connector). Serial ferrite beads for the RGB lines should have high frequency characteristics to eliminate relative noise. The 39 ohm series damping resistors for HSY and VSY should be placed near the D-SUB connector.

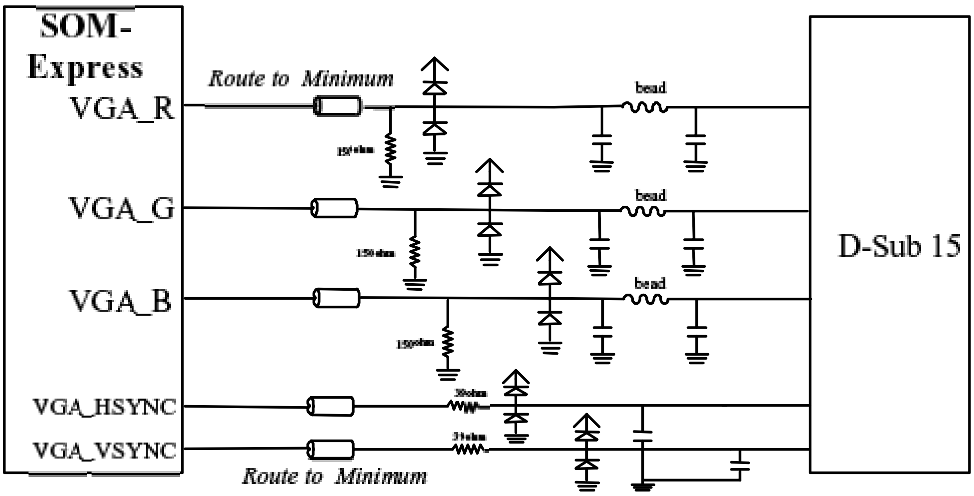


Figure 5-20 VGA Layout Guidelines

5.4.3.2 RGB Output Current Balance Path

Analog R, G and B (red, green and blue) traces should be designed to be as short as possible. Careful design, however, will allow considerable trace lengths with no visible artifacts. GNDRGB is an "analog current balance path" for the RGB lines. In terms of layout, GNDRGB should follow 2 traces that encapsulate the RGB traces all the way to the D-shell connector (VGA Port) and should not be tied to ground until connected to the Right Angle D-type connector.

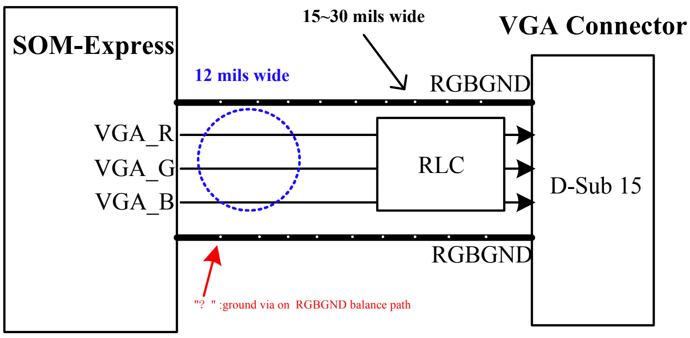


Figure 5-21 RGB Output Layout Guidelines

5.5 LVDS

5.5.1 Signal Description

Table 5-15 shows SOM-Express LVDS signals, including pin number, signals, I/0 and descriptions.

Table 5-15 LVDS signals description

Pin	Signal	I/O	Description
A71,73,75,78 A72,74,76,79	LVDS_A[0:3]+ LVDS_A[0:3]-	O	LVDS Channel A differential pairs
A81 A82	LVDS_A_CK+ LVDS_A_CK-	O	LVDS Channel A differential clock
B71,73,75,77 B72,74,76,78	LVDS_B[0:3]+ LVDS_B[0:3]-	O	LVDS Channel B differential pairs
B81 B82	LVDS_B_CK+ LVDS_B_CK-	O	LVDS Channel B differential clock
A77	LVDS_VDD_EN	O	LVDS panel power enable
B79	LVDS_BKLT_EN	O	LVDS panel backlight enable
B83	LVDS_BKLT_CTRL	O	LVDS panel backlight brightness control
A83	LVDS_I2C_CK	O	I2C clock output for LVDS display use
A84	LVDS_I2C_DAT	O	I2C data line for LVDS display use

5.5.2 Design Guideline

Figure 5-22 shows LVDS LCD connections.

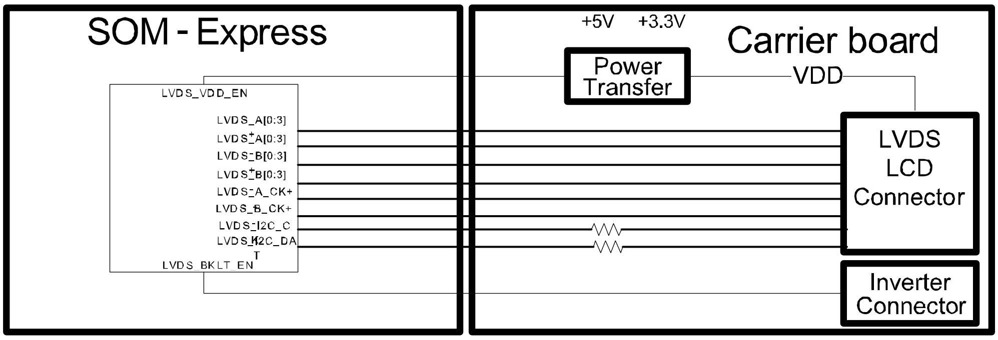


Figure 5-22 LVDS LCD Connections

5.5.2.1 Package Length Constraints

Skew minimization requires chipset die-pad to LVDS connector trace length matching of the LVDS signal pairs that belong to the same group including the clock strobe signals of that group. The reason for this is to compensate for the package length variation across each signal group in order to minimize timing variance. The chipset does not equalize package lengths internally, SOM-Express compensates for the mismatch length. Please be sure to be trace length matched on the carrier board. Table LV-2 shows the LVDS Signals Trace Length Mismatch Mapping.

Each LVDS signal should be trace length matched to its associated clock strobe within ±10 mils. The Channel A clock strobe pair must also be trace length matched to the Channel B clock strobe pair within ±10 mils.

Table 5-16 LVDS Signals Trace Length Mismatch Mapping					
Siganl group	**Data Pair**	**Signal matching**	**Clocks Associated with the channel**	**Clock Matching**	**Data To Associated Clock Matching**
CHANNEL A	LVDS_A[0]+ LVDS_A[0]-	±10 mils	LVDS_A_CK+ LVDS_A_CK-	±10 mils	±10 mils
	LVDS_A[1]+ LVDS_A[1]-	±10 mils			
	LVDS_A[2]+ LVDS_A[2]-	±10 mils			
	LVDS_A[3]+ LVDS_A[3]-	±10 mils			
CHANNEL B	LVDS_B[0]+ LVDS_B[0]-	±10 mils	LVDS_B_CK+ LVDS_B_CK-	±10 mils	±10 mils
	LVDS_B[1]+ LVDS_B[1]-	±10 mils			
	LVDS_B[2]+ LVDS_B[2]-	±10 mils			
	LVDS_B[3]+ LVDS_B[3]-	±10 mils			

5.5.3 Layout Requirements

Routing for LVDS transmitter timing domain signals for different traces terminated across 100Ω ± 15% and should be routed as follows.

- It is necessary to maintain the differential impedance, Zdiff = 100Ω ± 15%, where all traces are closely routed in the same area on the same layer.
- Isolate all other signals from the LVDS signals to prevent coupling from other sources onto the LVDS lines.
- The LVDS transmitter timing domain signals have maximum trace length of 10 inches. Be sure that the max trace length routed on the carrier board is 7.5 inches.
- Clocks must be matched to the associated data signals to within 10 mils.
- Channel-to-Channel clock length must be matched to within 10 mils.
- Minimum spacing between neighboring trace pair is 20 mils.
- Traces must be ground referenced.
- When choosing cables, it is important to remember that the differential impedance of cable should be 100Ω and the length must be less than 16 inches.

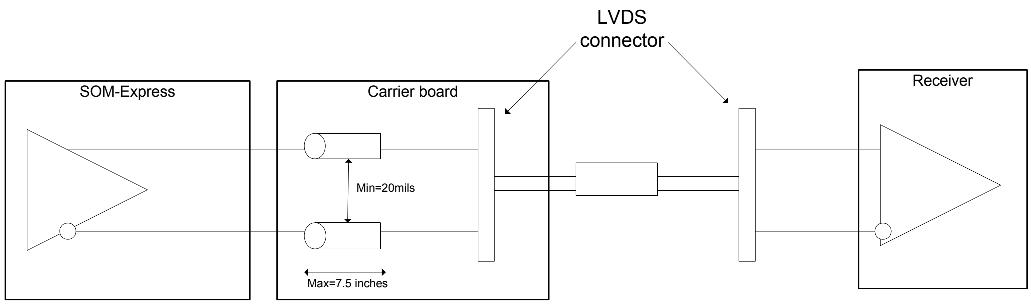


Figure 5-23 LVDS Signal Routing Topology

5.6 Primary IDE0

SOM-Express provides one IDE interface.

5.6.1 Signal Description

Table 5-17 shows SOM-Express IDE signals, including pin number, signals, I/0 and descriptions.

Table 5-17 IDE signals description

Pin	Signal	I/O	Description
-	IDE_D[0..15]	I/O	Bidirectional data to/from IDE device
D13,14,15	IDE_A[0..2]	O	Address lines to IDE device
D16	IDE_CS1#	O	IDE Device Chip Select for 1F0h to 1FF0h range
D17	IDE_CS3#	O	IDE Device Chip Select for 3F0h to 3FF0h range
D8	IDE_REQ	I	IDE DMA Request for IDE Master. This is the input pin from the IDE DMA request to do the IDE Master Transfer. It will active high in DMA or Ultra-33 mode and always be inactive low in PIO mode.
D10	IDE_ACK#	O	IDE device DMA Acknowledge
C13	IDE_IORDY	I	IDE device I/O ready input Pull low by the IDE device, active low
C14	IDE_IOR#	O	I/O ready line to IDE device
D9	IDE_IOW#	O	I/O write line to IDE device Data latched on trailing (rising) edge
D12	IDE_IRQ	I	Interrupt request from IDE device
D18	IDE_RESET#	O	Low active hardware reset (RSTISA inverted).
D77	IDE_CBLID#	O	Input from off-module hardware indicating the type of IDE cable being used. High indicates a 40-pin cable used for legacy IDE modes. Low indicates that an 80 pin cable with interleaved grounds is used. Such a cable is required for Ultra-DMA 66, 100 and 133 modes.

5.6.2 Design Guidelines

5.6.2.1 Design Considerations

The IDE port can support two hard drives or other ATAPI devices. The two devices on the port are wired in parallel, which is accomplished by plugging both drives into a single flat ribbon cable equipped with two socket connectors. A jumper is typically manually set on each device to set it for master or slave operation. If two devices are used in the master/slave mode on the same IDE port, the IDE_CBLID# pins of both devices must be connected together. These pairs of pins negotiate between the master and slave devices. The devices may not function correctly unless these pins are interconnected. If two devices are plugged into a single IDE cable, the cable will interconnect the pins properly. If the two devices on one port are integrated on the carrier board or plugged into separate connectors, care should be taken to tie the corresponding pins together.

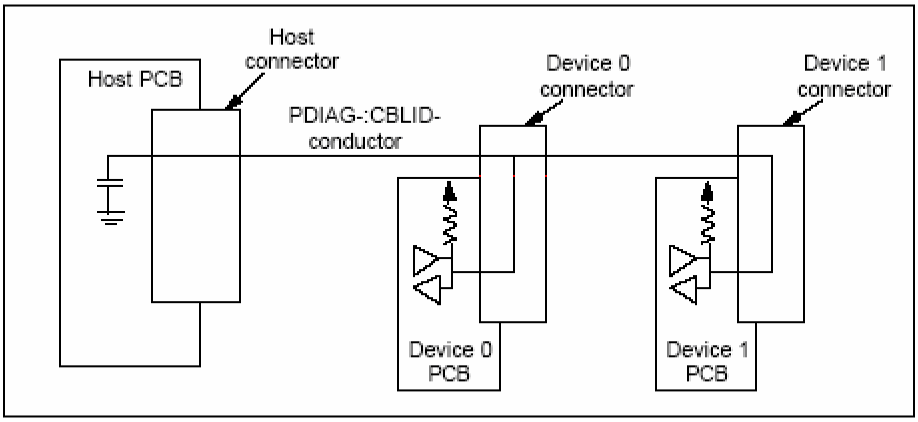


Figure 5-24 IDE Master/Slave Handshake Signals Connection

5.6.2.2 UDMA Support

Some SOM-Express modules support UDMA 33 data transfer mode. If an advanced IDE data transfer mode such as UDMA 66 is required, it requires a special 80-conductor IDE cable for signal integrity.
For UDMA 66 support, it is recommended the IDE bus and total cable length of carrier board do not exceed 13 inches.

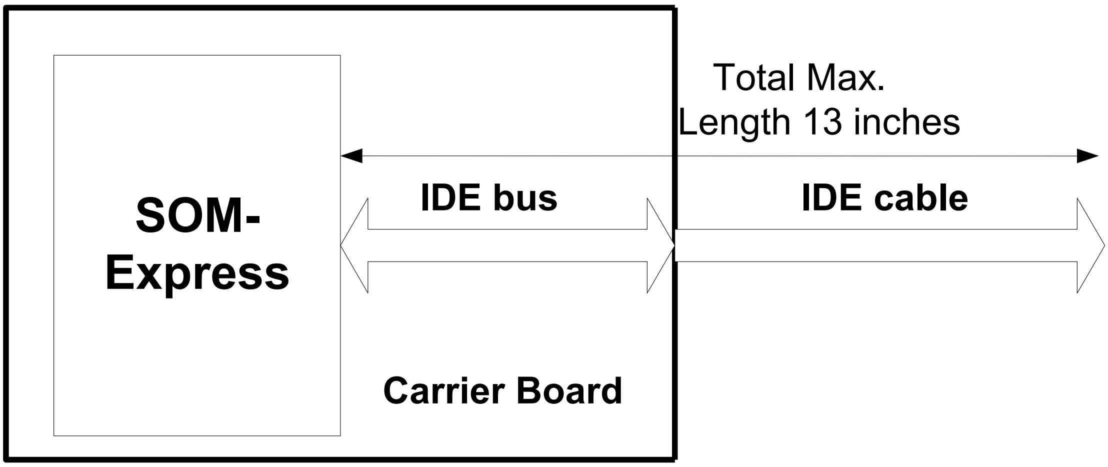


Figure 5-25 IDE Bus Trace on Carrier Board and Cable

5.6.2.3 IDE interface connections

All necessary pull up/down resistors are implemented on the SOM module and do not need to be implemented on the carrier board.

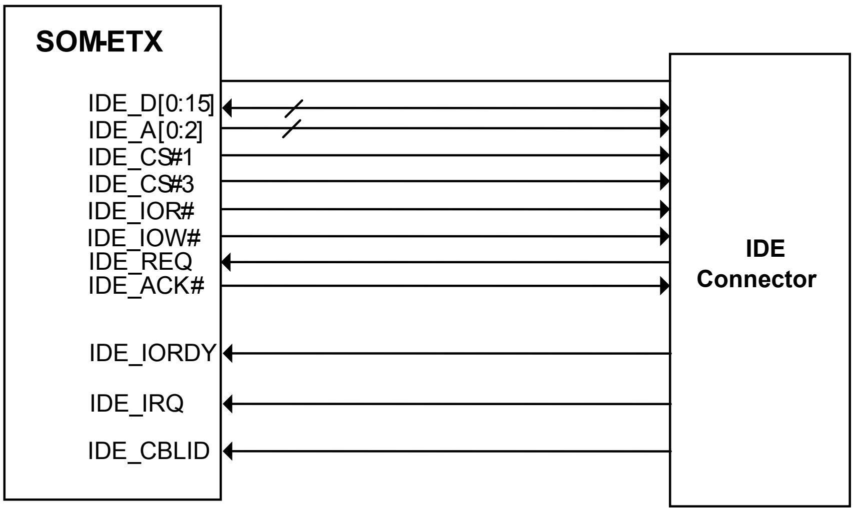


Figure 5-26 IDE0 Connections

5.6.2.4 CompactFlash Socket Implementation Notes

The CompactFlash (CF) card cannot be hot-plugged (changed while the system is powered). If hot-plug support is necessary, then a PCI-based CardBus controller chip can be integrated onto the carrier board and used to control the CF socket. The CF card can be configured as a slave device when the CSEL signal is set as non-connection. If two CF cards (or a CF card and a hard drive) are used in the master/slave mode on the same IDE port, the IDE_CBLID# pins on both devices must be connected. These pins negotiate between the master and slave devices. The devices may not function correctly unless these pins are interconnected.

5.6.3 Layout Guidelines

5.6.3.1 IDE data and strobe routing guideline

This section contains guidelines for connecting and routing the IDE interface. SOM-Express provides one independent IDE channel. This section provides guidelines for IDE connector cabling and carrier board design. Additional external 0 Ω resistors can be incorporated into the design to address possible noise issues on the carrier board. If used, these resistors should be placed close to the connector.

The IDE interface can be routed with 6-mil traces on 6-mil spaces (dependent upon stack-up parameters), and must be less than 10 inches long (from SOM-Express connector to carrier board IDE connector). Additionally, the maximum length difference between the data signals and the strobe signal of a channel is 450 mils.

Table 5-18 IDE Routing Summary

Trace Impedance	IDE Routing requirements	Trace length	IDE Signal length matching
55 Ω ± 15%	6 on 6 (Based on stack-up in chap 4)	1 ~ 10 inches	The two strobe signals must be matched within 100 mils of each other. The data lines must be within ± 450 mils of the average length of the two strobe signals

5.7 Ethernet

SOM-Express supports the IEEE802.3 network interface and flexible dynamically loadable EEPROM algorithm. The network interface complies with the IEEE standard for 10BASE-T, 100BASE-T and 1000BASE-T Ethernet interfaces.

5.7.1 Signal Descriptions

Table 5-19 shows SOM-Express Ethernet signals, including pin number, signals, I/0, power plane and descriptions.

Table 5-19 Ethernet signal description

Pin	Signal	I/O	Description
A13,A9,A7,A3 A12,A10,A6,A2	GBE0_MDI[0:3]+ GBE0_MDI[0:3]-	I/O	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some mode, per the following: 1000BASE-T 100BASE-TX 10BASE-T MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-
B2	GBE0_ACT#	OD	Gigabit Ethernet Controller 0 activity indicator, active low.
A8	GBE0_LINK#	OD	Gigabit Ethernet Controller 0 link indicator, active low.
A4	GBE0_LINK100#	OD	Gigabit Ethernet Controller 0 100 Mbit / sec link indictor, active low.
A5	GBE0_LINK1000#	OD	Gigabit Ethernet Controller 0 1000 Mbit / sec link indictor, active low.
A14	GBE0_CTREF	REF	Reference voltage for Carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module PHY and may be as low as 0 V and as high as 3.3 V. The reference voltage output shall be current limited on the module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less.

5.7.2 Design Guidelines

5.7.2.1 Differential Pairs

Route the transmit and receive lines on the input (SOM-Express module) side of the coupling transformer on the carrier board PCB as differential pairs, with a differential impedance of 100 Ω. PCB layout software allows determination of the correct trace width and spacing to achieve this impedance after the PCB stack-up configuration is known.

With 10/100M, the TX+, TX- signal pair should be well separated from the RX+, RX- signal pair. Both pairs should be well separated from any other signals on the PCB. The total routing length of these pairs from the SOM-Express module to the Ethernet jack should be made as short as practical. If the carrier board layout doesn't specify where the Ethernet jack is located, it should be placed close to the SOM-Express module pins.

Figure 5-27 and Figure 5-28 shows the 10/100M Ethernet and Gigabit Ethernet Connections.

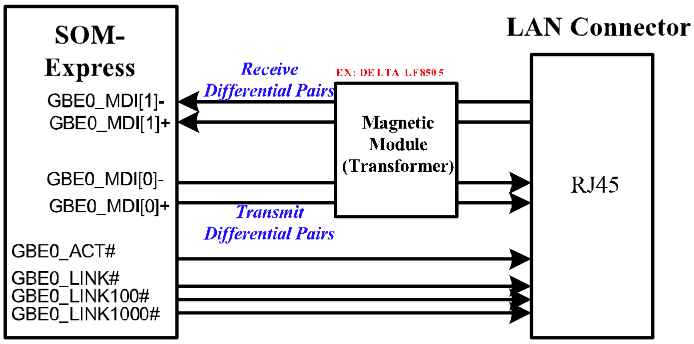


Figure 5-27 10/100M Ethernet Connections

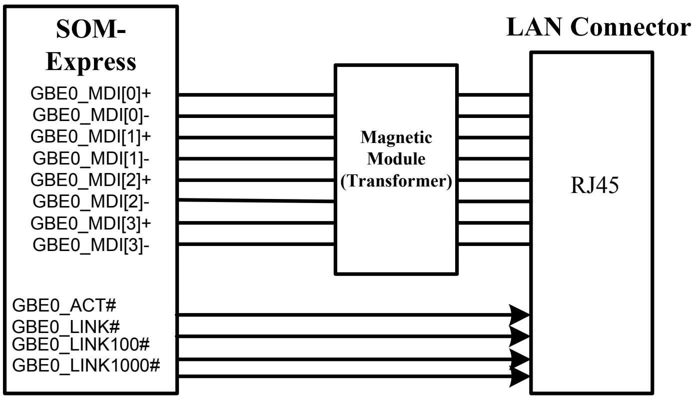


Figure 5-28 Gigabit Ethernet Connections

5.7.2.2 Power Considerations and Ethernet LED

In general, any section of traces that are intended for use with high-speed signals should observe proper termination practices. Many board layouts remove the ground plane underneath the transformer and the RJ-45 jack to minimize capacitive coupling of noise between the plane and the external Ethernet cable. Figure 5-29 shows an example.

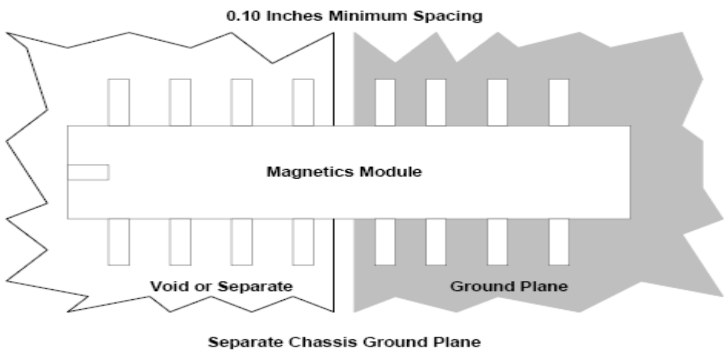


Figure 5-29 Ground Plane Separation

5.7.2.3 Implementation of indicators

Some RJ-45 include LEDs which need 3.3 volts to drive the link and action LEDs, so we need to provide 3.3 volts on the carrier board. Link and activity LEDs can be implemented by using the SOM-Express module's GBE0_ACT#, GBE0_LINK#, GBE0_LINK100#, and GBE0_LINK1000# pins. These pin's sink current is intended for attachment to a LED cathode. The anode of the LED should be pulled to 3.3 volts through a resistor of 220 Ω or greater.

5.7.3 Layout Guidelines

Critical signal traces should be kept as short as possible to decrease the likelihood of being affected by high frequency noise from other signals; including noise carried on power and ground planes. Keeping the traces as short as possible can also reduce capacitive loading.
Designing for gigabit operation is very similar to designing for 10/100 Mbps. 10/100Mbps has two differential pairs, but can be generalize for a gigabit system with four analog pairs.

5.7.3.1 Differential pairs design considerations

- Maintain constant symmetry and spacing between the traces within a differential pair. Keep the signal trace lengths of a differential pair equal to each other. Do not use serpentines to try to match trace lengths in the differential pair. Serpentines cause impedance variations causing signal reflections, which can be a source of signal distortion. Try to keep the length difference of the differential pair less than 100 mil (~15 pS). Always go straight to the required via or pad.

- The total length of each differential pair should be less than 4 inches. There is 1.5 inches on SOM-Express, so keep the length of each differential pair under 2.5 inches. Figure 5-30 shows an example. L1 is 1.5 inches on the SOM-Express. On your carrier board, L2 should be less than 2.5 inches.

- Do not route the transmit differential traces closer than 100 mils to the receive differential traces for 10/100 Mbps.

- Do not route any other signal traces (including other differential pairs) parallel to the differential traces or closer than 100 mils to the differential traces. Figure 5-30 shows an example. We recommend length L3 to be kept longer than 100 mils.

- Separate traces within a differential pair as small as possible down to 5 to 8 mils. Close separation of the traces allow the traces to couple well to each other.

- For high-speed signals, it should minimize the number of corners and vias. If a 90° bend is required, it is recommended to use two 45° bends instead. Please see Figure 5-31 for an example.

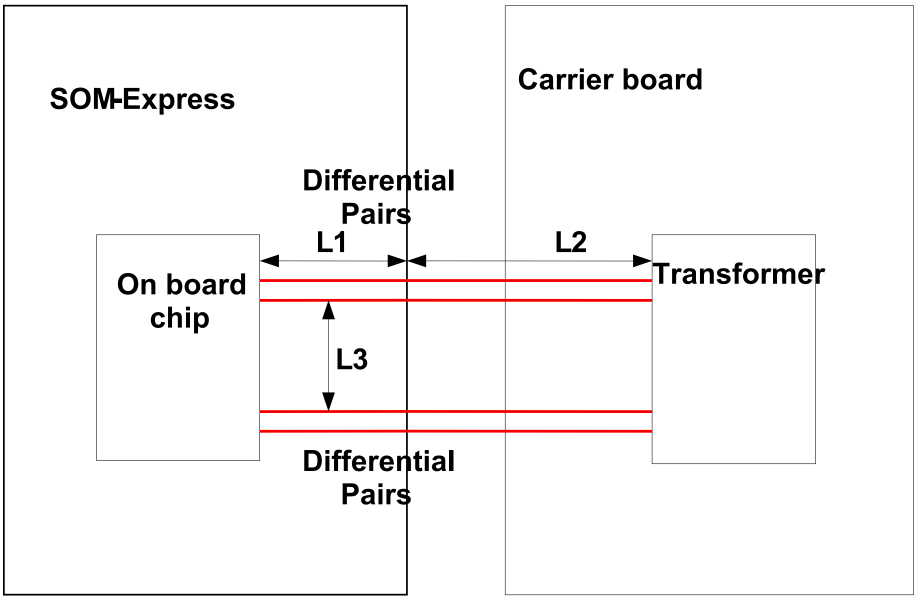


Figure 5-30 Differential signals route example

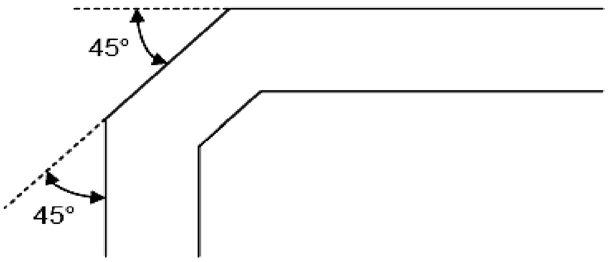


Figure 5-31 Bend example

5.7.3.2 Transformer

We recommend using the integrated Magnetic Modules/RJ-45 connectors. If using the discrete Magnetic Modules and RJ-45 connector, the transformer should be placed close to the RJ-45 connector to limit EMI emissions. Each differential pair of data signals is required to be parallel to each other with the same trace length on the component (top) layer and to be parallel to a respective ground plane. The 49.9 Ω pull-down resistors for each differential pair are suggested to be located as close to the transformer as possible. Figure 5-32 and 5-33 show the 10/100M and Gigabit Ethernet Layout guidelines.

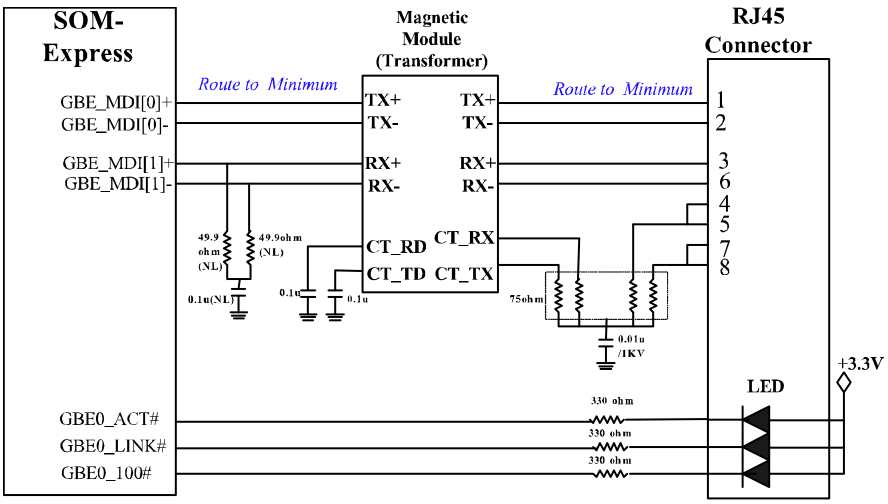


Figure 5-32 10/100M Ethernet Interconnection

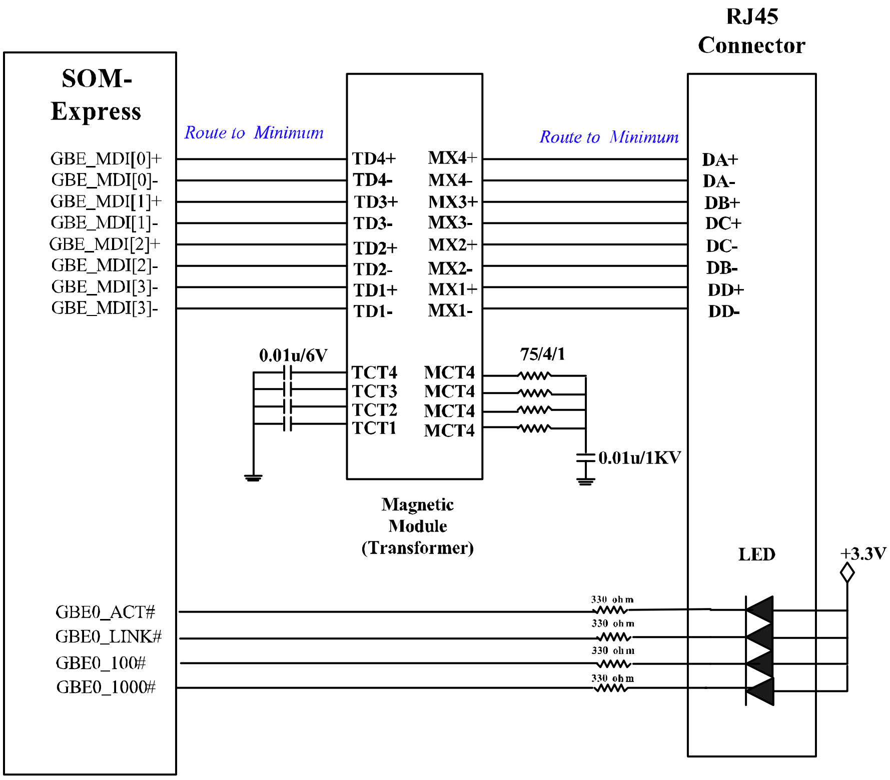


Figure 5-33 Gigabit Ethernet Interconnection

5.7.3.3 Critical Dimensions

There are two critical dimensions that must be considered during the layout phase of an Ethernet controller. These dimensions are identified in Figure 5-34 as A and B.

Distance A: Transformer to RJ-45 (Priority 1). The distance labeled A should be given the highest priority in the backplane layout. The distance between the transformer module and the RJ-45 connector should be kept to less than 1 inch of separation. The following trace characteristics are important and should be observed:

1. Differential Impedance: The differential impedance should be 100 Ω. The single ended trace impedance will be approximately 50 Ω; however, the differential impedance can also be affected by the spacing between the traces.

2. Trace Symmetry: Differential pairs should be routed with consistent separation and with exactly the same lengths and physical dimensions (for example, width).

Distance B: SOM-Express to Transformer (Priority 2)
Distance B from Figure 5-34 should also be designed to extend as short as possible between devices, be sure not to go over 2.5 inches. The high-speed nature of the signals propagating through these traces requires that the distances between these components be closely observed.

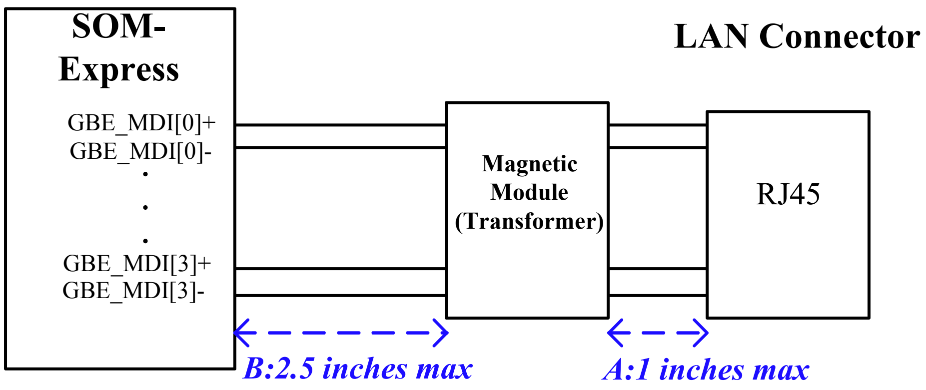


Figure 5-34 Critical Dimensions

5.8 TV-Out

The TV-out display (TV DAC) interface consists of 3 outputs which can be used in different combinations to support component video, S-video or composite video.

5.8.1 Signal Descriptions

Table 5.20 TV signals description			
Pin	**Signal**	**I/O**	**Description**
B97	TV_DAC_A	O	TVDAC Channel A Output supports the following: Composite video: CVBS Component video: Chrominance (Pb) analog signal S-Video: not used
B97	TV_DAC_B	O	TVDAC Channel B Output supports the following: Composite video: not used Component video: Luminance (Y) analog signal S-Video: Luminance analog signal
B97	TV_DAC_C	O	TVDAC Channel C Output supports the following: Composite video: not used Component video: Chrominance (Pr) analog signal S-Video: Chrominance analog signal

5.8.2 Design Guidelines

5.8.2.1 Termination resistor, output filter and ESD protection diodes of TV DAC output

There are three DAC output pins: TV_DAC_A, TV_DAC_B, and TV_DAC_C.
One of the 150 Ω ± 1% parallel termination resistors is implemented on the SOM-Express module. Please place another 150 Ω ± 1% parallel termination resistor, a set of protection diodes (like BAT54S) and an output network filter on the carrier board. The video output signals should overlay the ground plane and be separated by a ground trace, inductors and ferrite beads in series.
Figure 5-35 shows the connection of TV-out.

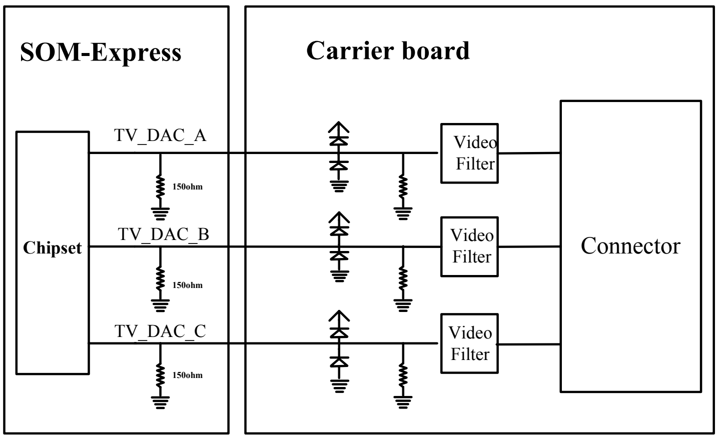


Figure 5-35 Connection of TV-out

5.8.2.2 ESD diode

ESD diodes are required for each TV DAC channel output. The diodes should connect between the 3.3 V power plane (from the regulator) and ground. These diodes should have a low C rating (~ 5 pF max) and a small leakage current (~ 10 uA at 120℃).The diodes should be placed to keep the inductance of the 3.3 V power rail connection as low as possible. The diode placement should be similar for all three channel outputs and should not be shared with any other signals, especially video or clock signals. In addition, one decoupled capacitor, C1= 0.1 uF, should be placed in close proximity and across the ESD diodes to reduce noise on the 3.3 V rail.

5.8.2.3 TV DAC Video Filter

A video filter is required for each TV DAC channel output signal. This video filter is to be placed in close proximity to the connector. The separation between each of the 3 video filters for the TV DAC channels should be a minimum of 50 mils or greater if possible in order to minimize crosstalk. This is especially important for the TVDAC_B and TVDAC_C channels (S-video signals). Figure 5-36 shows the TV DAC Video Filter.

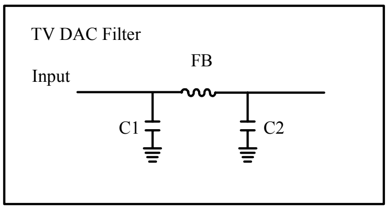


Figure 5-36 TV DAC Video Filter

The video filter is designed for a cutoff frequency of at least 30 MHz and a gain of -3 dB. Table 5-21 shows the TV DAC Video Filter component descriptions.

Table 5-21 TV DAC Video filter component descriptions

Component	Value	Tolerance	Voltage/Current	Type
C1	6 pF	± 20%	16 V	Ceramic
C2	6 pF	± 20%	16 V	Ceramic
FB	150 Ω@ 100 MHz	± 25%	100 mA	

5.8.3 Layout Guidelines

5.8.3.1 TV DAC routing

The minimum spacing between each TV DAC signal is 40 mils, but 50 mils is preferred. A maximum amount of spacing should be used between each TV DAC signal as well as to all other toggling signals. This helps prevent crosstalk between the TV DAC signals and other toggling signals. The routing for each TV DAC signal should also be matched and balanced as much as possible. All TV DAC signals should be routed on the same layer, have a similar number of bends, the same number of vias, etc. All routing should be done with ground referencing as well. Figure 5-37 shows the TV DAC routing Topology.

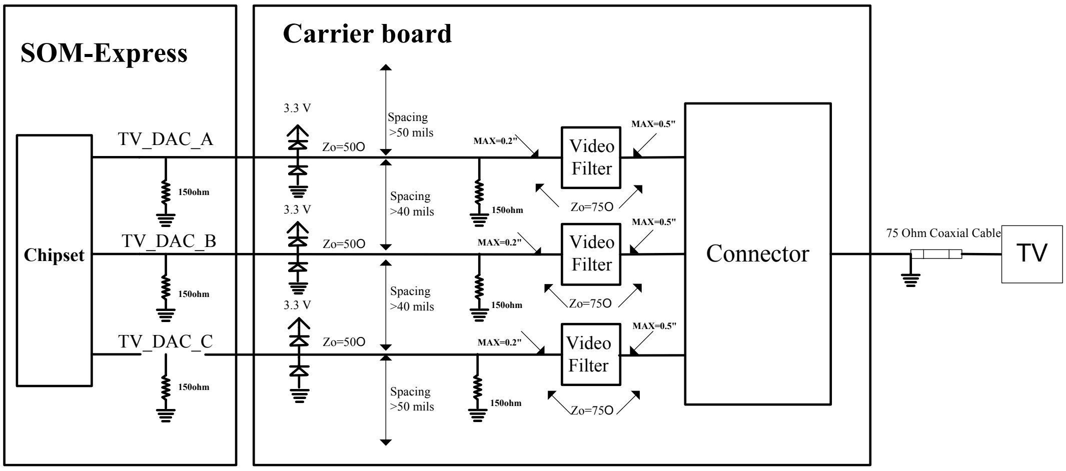


Figure 5-37 TV DAC Routing Topology

5.9 Miscellaneous

5.9.1 Miscellaneous Signal Descriptions

Table 5.22 Miscellaneous signal descriptions			
Pin	**Signal**	**I/O**	**Description**
B32	SPKR	O	This is the PC speaker output signal from the SOM-Express module. Please connect this signal to the speaker.
B33	I2C_CK	O	General purpose I2C port clock output.
B34	I2C_DAT	I/O OD	General purpose I2C port data I/O line.
A34	BIOS_DISABLE#	I	Module BIOS disable input. Pull low to disable module BIOS. Used to allow off-module BIOS implementations.
B27	WDT	O	Output indicating that a watchdog time-out event has occurred.
A86	KBD_RST#	I	Input to module from (optional) external keyboard controller that can force a reset. Pulled high on the module. This is a legacy artifact of the PC-AT.
A87	KBD_A20GATE	I	Input to module from (optional) external keyboard controller that can be used to control the CPU A20 gate line. The A20GATE restricts memory access to the bottom megabyte and is a legacy artifact of the PC-AT. Pulled low on the module.
A93,B54 B57,B63	GPO[0:3]	O	General purpose output pins. Upon hardware reset, these outputs should be low.
A54,A63 A67,A85	GPI[0:3]	I	General purpose input pins. Pulled high internally on the module.
B13	SMB_CK	I/O OD	System Management Bus bidirectional clock line. Power sourced through 5 V standby rail and main power rails.
B14	SMB_DAT	I/O OD	System Management Bus bidirectional data line. Power sourced through 5 V standby rail and main power rails.
B15	SMB_ALERT#	I	System Management Bus Alert – active low input can be used to generate a SMI# (System Management Interrupt) or to wake the system. Power sourced through 5 V standby rail and main power rails.
C54 C57 D57	TYPE[0:2]#	PDS	The TYPE pins indicate to the Carrier Board the Pin-out Type that is implemented on the module. The pins are tied on the module to either ground (GND) or are no-connects (NC). For Pin-out Type 1, these pins are don't care (X).

			TYPE2# TYPE1# TYPE0# X X NC Pin-Out Type 1 NC NC GND Pin-Out Type 2 NC NC NC Pin-Out Type 3 (no IDE) NC GND GND Pin-Out Type 4 (no PCI) NC GND NC Pin-Out Type 5 (no IDE,PCI) The Carrier Board should implement combinatorial logic that monitors the module TYPE pins and keeps power off (e.g. deactivates the ATX_ON signal for an ATX power supply) if an incompatible module pin-out type is detected. The Carrier Board logic may also implement a fault indicator such as an LED.
B12	PWRBTN#	I	Power button to bring system out of S5 (soft off), active on rising edge.
B49	SYS_RESET#	I	Reset button input. Active low input. System is held in hardware reset while this input is low, and comes out of reset upon release.
B50	CB_RESET#	O	Reset output from module to Carrier Board. Active low. Issued by module chipset and may result from a low SYS_RESET# input, a low PER_OK input, a VCC_12V power input that falls below the minimum specification, a watch dog timeout, or may be initiated by the module software.
B24	PWR_OK	I	Power OK from main power supply. A high value indicates that the power is good
B18	SUS_STAT#	O	Indicates system suspend operation; used to notify LPC devices.
A15	SUS_S3#	O	Indicates system is in Suspend to RAM state. Active low output.
A18	SUS_S4#	O	Indicates system is in Suspend to Disk state. Active low output.
A24	SUS_S5#	O	Indicates system is in Soft Off state. Also known as “PS_ON” and can be used to control an ATX power supply.
B66	WAKE0#	I	PCI Express wake up signal.
B67	WAKE1#	I	General purpose wake up signals. May be used to Implement wake-up on PS2 keyboard or mouse activity.
A27	BATLOW#	I	Indicates that external battery is low.
B35	THRM#	I	Input from off-module temp sensor indicating an over-temp situation.
A35	THRMTRIP#	I	Active low output indicating that the CPU has entered thermal shutdown.

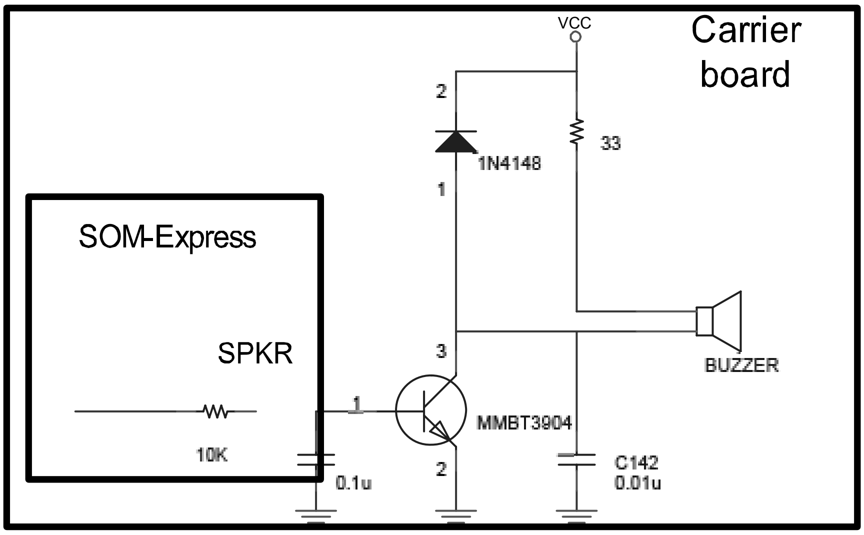


Figure 5-38 Speaker Connections

The SPKR output from the SOM-Express module is a CMOS level signal. It can control an external FET or logic gate that drives an external PC speaker. The SOM-Express modules SPKR output should not be directly connected to either a pull-up or a pull-down resistor. The SPKR signal is often used as a configuration strap for the core chipset in SOM-Express modules. A pull-up or pull-down on this signal can override the internal setting in the module and result in malfunction of the module.

5.9.2 I2C Bus

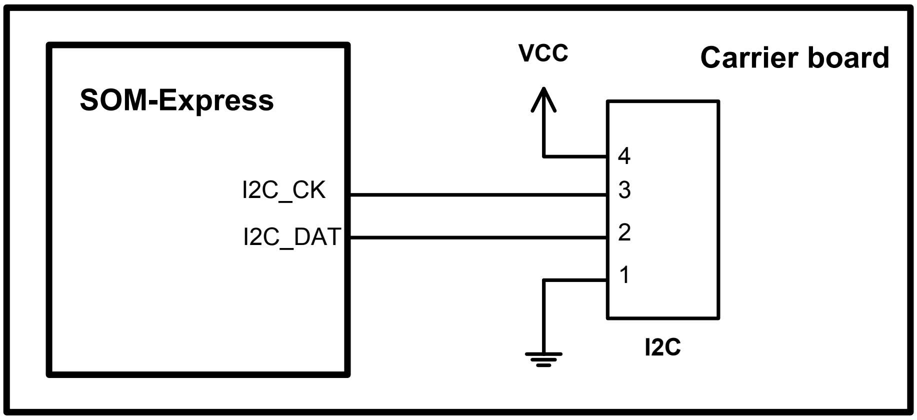


Figure 5-39 I2C Bus Connections

Most SOM-Express modules provide a software-driven I2C port for communication with external I2C slave devices. This port is implemented on SOM-Express Pins I2C_DAT and I2C_CK.

5.9.3 SMBus

Most SOM-Express modules provide a SMBus port for communication with external SMBus slave devices. This port is also used internally in the SOM-Express module to communicate with onboard SMBus devices such as the SPD EEPROMs on DIMMS, clock-generator chips, and hardware monitoring devices. The port is externally available on the SOM-Express pins SMB_DAT and SMB_CK. The addresses for any external SMBus devices must be chosen so that they do not conflict with the addresses that are used internally in the SOM-Express module. If the device offers externally controllable address options, it is desirable to implement carrier board resistor straps to allow the device to be set to at least two possible SMBus addresses.

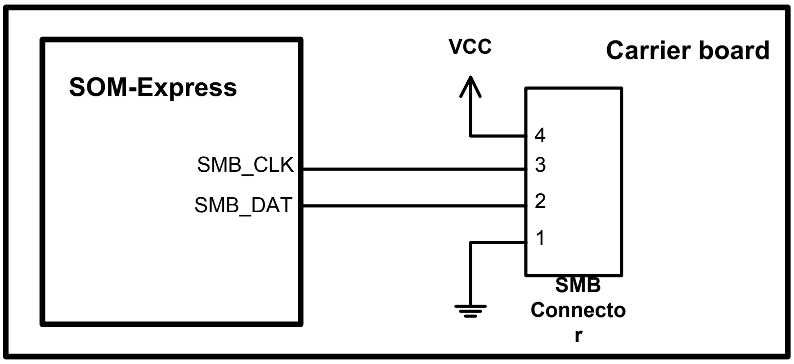


Figure 5-40 SMB Bus Connections

5.9.4 Power Good/Reset Input

The SOM-Express Power OK Input (PWR_OK) may be attached to an external power good circuit if desired, or used as a manual reset input by grounding the pin with a momentary-contact pushbutton switch. If an external circuit asserts this signal, it should be driven by an open-drain driver and held low for a minimum of 15mS to initiate a reset. Use of this input is optional. The SOM-Express module generates its own power-on reset based on an internal monitor on the +5 V input voltage and/or the internal power supply.

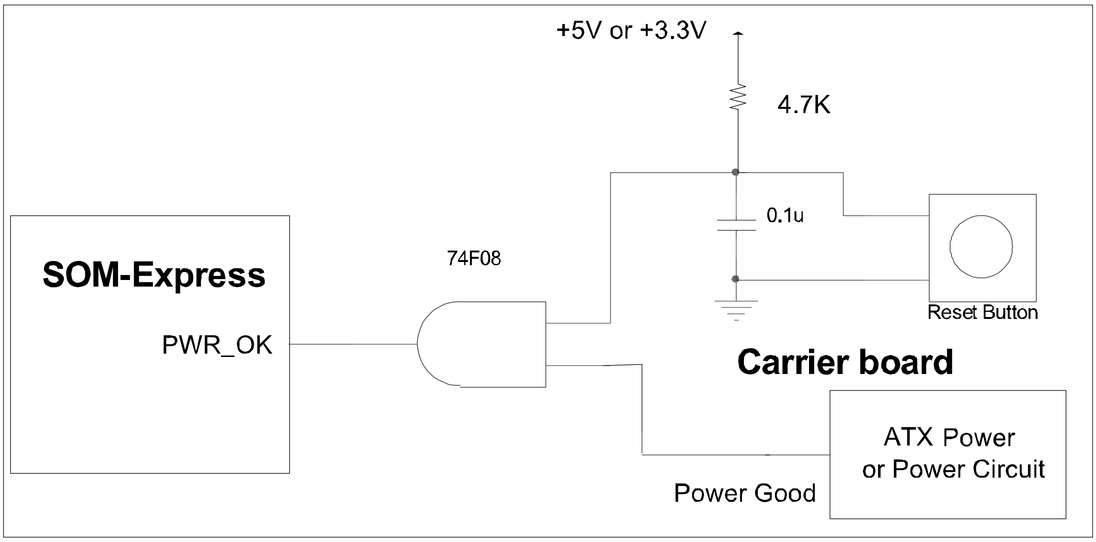


Figure 5-41 Power OK/Reset Input Connections

5.9.5 WDT

SOM-Express provides a watch-dog function via the pin WDT. It can prevent the system from shutting down for a long time. It can generate a signal to reset the system. In SOM-Express, the WDT is low active. Figure 5-42 shows an example of the watch-dog circuit.

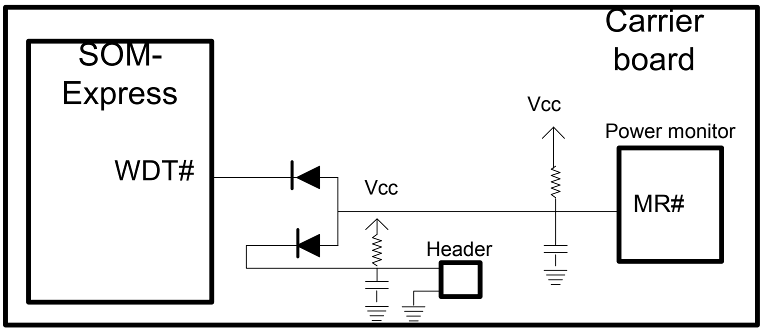


Figure 5-42 Example of a watch-dog circuit

5.10 PCI Express Bus

SOM-Express provides a PCI Express Bus interface that is compliant with the PCI Express* Base Specification, Revision 1.0a. It supports several general purpose PCI Express port (x1) and external graphics using PCI Express architecture (x16). For more information on the PCI Express Bus interface, refer to the PCI Express* Base Specification, Revision 1.0a.

5.10.1 Signal Description

Table 5-23 shows SOM-Express PCI Express bus signals for general purpose, Table 5-24 shows PCI Express bus signal for external graphics. Table 5-25 shows ExpressCard Support signals. Each table includes pin number, signals, I/0, and descriptions.

Table 5-23 PCIE Signal Description(General purpose)

Pin	Signal	I/O	Description
A68,64,61,58,55,52 A69,65,62,59,56,53	PCIE_TX[0:5]+ PCIE_TX[0:5]-	O	PCI Express Differential Transmit Pairs 0 through 5
B68,64,61,58,55,52 B69,65,62,59,56,53	PCIE_RX[0:5]+ PCIE_RX[0:5]-	I	PCI Express Differential Receive Pairs 0 through 5
-	PCIE_TX[16:31]+ PCIE_TX[16:31]-	O	PCI Express Differential Transmit Pairs 16 through 31 These are same line as PEG_TX[0:15]+ and -
-	PCIE_RX[16:31]+ PCIE_RX[16:31]-	I	PCI Express Differential Receive Pairs 16 through 31 These are same line as PEG_TX[0:15]+ and -
A88 A89	PCIE_CLK_REF+ PCIE_CLK_REF-	O	Reference clock output for all PCI Express Graphics lanes.
B66	WAKE0#	I	PCI Express wakeup signal.

Table 5-24 PEG Signal Description(x16 Graphics)

Pin	Signal	I/O	Description
-	PEG_TX[0:15]+ PEG_TX[0:15]-	O	PCI Express Graphics Transmit Differential Pairs 0 through 15 Some of these are multiplexed with SDVO lines.
-	PEG_RX[0:15]+ PEG_RX[0:15]-	I	PCI Express Graphics Receive Differential Pairs 0 through 15 Some of these are multiplexed with SDVO lines.
D54	PEG_LANE_RV#	I	PCI Express Graphics lane reversal input strap. Pull low on the carrier board to reverse lane order. Be aware that the SDVO lines that share this interface do not necessarily reverse order if this s strap is low.
D97	PEG_ENABLE#-	I	Strap to enable PCI Express x16 external graphics interface. Pull low to disable internal graphics and enable the x16 interface.

Table 5-25 Express Card Support

Pin	Signal	I/O	Description
A49,B48	EXCD[0:1]_CPPE#	I	PCI ExpressCard: PCI Express capable card request, active low, one per card
A48,B47	EXCD[0:1]_RST#	O	PCI ExpressCard: reset, active low, one per card

5.10.2 Design Guidelines

5.10.2.1 PCI Express AC Coupling Capacitor

Each PCI Express lane is AC coupled between its corresponding transmitter (TX) and receiver (RX). Figure 5-43 shows the connection for SOM-Express PCI Express signals. It is best to place AC coupling capacitors close to the transmitter (TX) of the SOM-Express board.

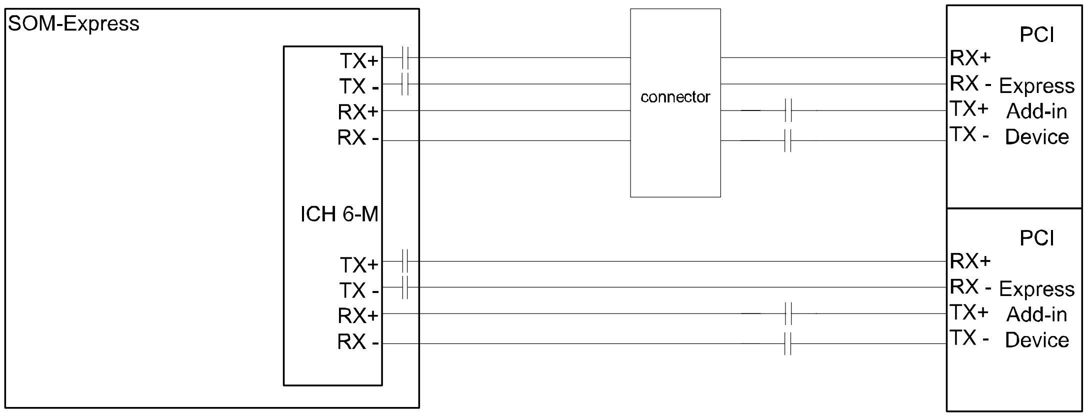


Figure 5-43 PCI Express Interconnect Example

We recommend using size 0603 capacitors. Use the exact same package size for the capacitor on each signal in a differential pair. Table 5-25 shows the PCI Express capacitor summary.

Table 5-26 PCI Express Capacitor Summary

Type	Value	Tolerance	Placement	Length Matching Between Differential Pair
AC Capacitor	75 nF-200 nF	20%	Recommended to place close to the transmit side	As close as possible between the differential pairs

5.10.2.2 Bowtie Topology Considerations: Untangling Nets

It is possible that when interconnecting PCI Express devices, certain “bowtie” or signal-crossing scenarios might occur when the link is routed on the PCB. There are three main types of bow tie scenarios:

(1) TX+, TX- crisscrossing within a pair.
(2) Crossing of transmitter and receiver pairs within a lane.
(3) Crossing of lanes within a link.

The PCI Express specification provides two different features: Polarity Inverse and Lane Reversal to help system designers overcome the layout difficulties encountered in scenarios #1 and #3. The specification does not include any provisions to address scenario #2

- **Polarity Inversion**

The PCI Express spec requires polarity inversion to be supported independently by all receivers across the link, i.e. the positive signal from the transmitter (TX+) can connect to the negative signal of the receiver (RX-) in the same lane. Of course that means the negative signal from the transmitter (TX-) must now also connect to the positive signal of the receiver (RX+) in such a scenario. Figure 5-44 shows an example. But be careful, it is important that polarity inversion does not direction inversion, i.e. the TX differential pair from one device must still connect to the RX differential pair on the receiver device.

Figure 5-44 Polarity Inversion on a TX to RX Interconnect

- **Lane Reversal**

Lane reversal allows the lane number to be switched from high to low and low to high. For example the lane 15 from the SOM-Express would connect to lane 0 of the device, and lane 0 from the SOM-Express would connect to lane 15 of the device. Lane reversal need only be supported by one of the devices in the link to allow its implementation. It is important to note that similar to polarity inversion, Lane Reversal does not imply direction reversal, i.e. the TX differential pair from an upstream device must still connect to the RX differential pair on the downstream device. Figure 5-45 shows an example.

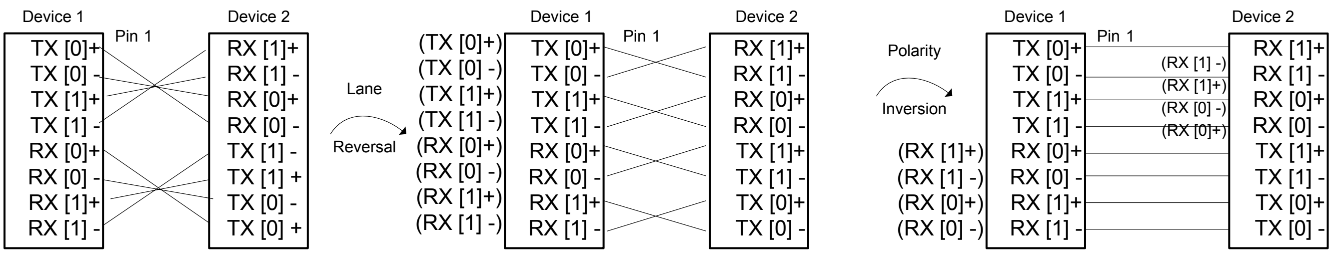


Figure 5-45 Lane Reversal and Polarity Inversion - TX to RX Interconnect

Note: Lane Reversal is not supported for multiplexed SDVO signals on the external graphics using the PCI Express architecture interface.

5.10.2.3 Terminating Unused PCI Express Ports

If a PCI Express port will not be implement on the platform, the PCIE _TX+/-[x] and PCIE_RX+/-[x] signals may be left as No Connects.

Note: Where “x” is the port number left as No Connect.

If no PCI Express ports will be implemented on the platform, the PCIE _TX+/- [0:5] and PCIE _RX+/- [0:5] signals may be left as No Connect and the WAKE# signal should be pulled-up to VccSus 3_3 with a 680 Ω – 1 kΩ resistor. Figure 5-46 shows the circuit.

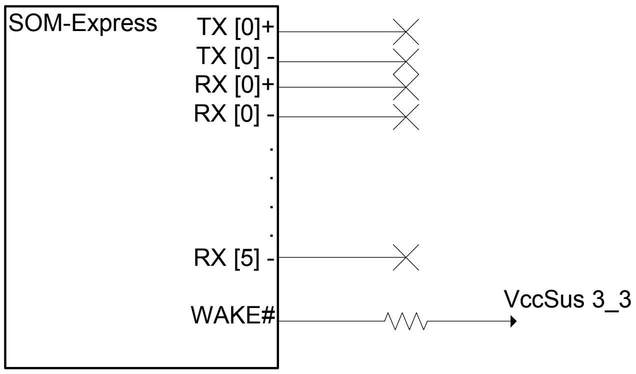


Figure 5-46 Example of terminating unused PCI Express ports

5.10.3 Layout Guidelines

The following represents a summary of the layout and routing guideline.

5.10.3.1 Differential pairs

The PCI Express signals should be routed as differential pairs. The following is a summary of general routing guidelines for the differential pair traces.

In SOM-Express platforms the PCI Express differential trace impendence target is 100 Ω ± 20%.

It is important to equalize the total length of the traces in the pair throughout the trace; each segment of trace length should be equal along the entire length of the pair. Figure 5-47 shows an example. L_A must equal to L_A', L_B must equal to L_B'…, and so on.

It is preferable to route TX and RX differential pairs alternately on the same layer (TX pair next to RX pair rather than another TX pair).

Tight coupling within the differential pair and increased spacing to other differential pairs helps to minimize EMI and crosstalk.

It is important to maintain routing symmetry between the two signals of a differential pair.

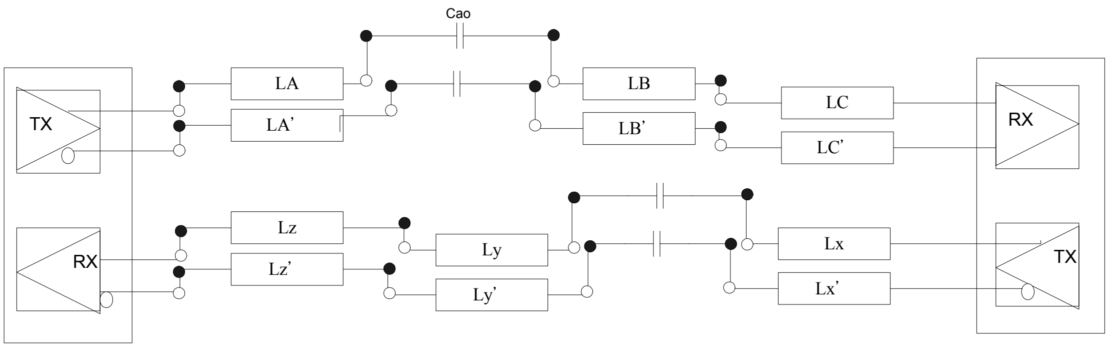


Figure 5-47 Line equalization

5.10.3.2 Board Stack-up Considerations

Table 5-27 shows the PCI Express Trace Width and Spacing for Micro-strip and Strip-line base on the six layer board stack-up. Please refer to chapter 4 to get more information. Keep the required impedance based on the different board stack-up.

Table 5-27 PCI Express Trace Width and Spacing for Micro-strip and Strip-line

	Trace Width	Differential Pair Trace Spacing	Adjacent Pair / Trace Spacing	Differential Pair Length Matching	Breakout Guideline	Nominal Trace Impedance (Zo)
Micro-strip	5 mils	6 mils	20 mils	5 mils	5 mil trace width, 5mil separation to both the differential pair signals and adjacent traces for up to 250 mils	100 Ω±20% (Differential)
Strip-line	4 mils	8 mils	20 mils	5 mils	Only 4 mil trace width on 8 mils spacing is allowed	100 Ω±20% (Differential)

5.10.3.3 PCI Express Topology #1 – Device Down Routing Guidelines

The device down topology allows a maximum of 15 inches from SOM-Express pin to the pin of the down device. This max length takes into account all routing, including the breakout region, which should not exceed 0.25 inches per device. The TX and RX pairs can be routed "interleaved", such that the pairs alternate between TX and RX on the carrier board, or "non-interleaved", where TX and RX pairs are routed next to each other. Only interleaved routing can used for microstrip routing topologies. For stripline routing, It is preferable to route the TX and RX differential pairs in an interleaved fashion to reduce crosstalk. Figure 5-48 shows the example.

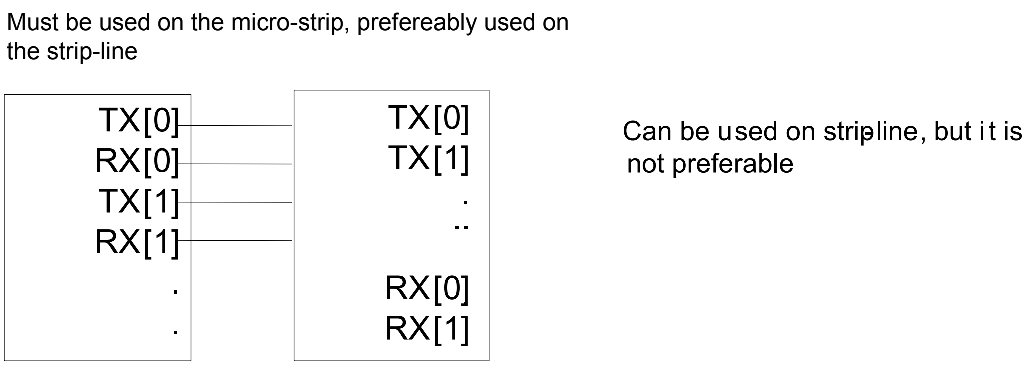


Figure 5-48 Example of "interleaved" and "non-interleaved"

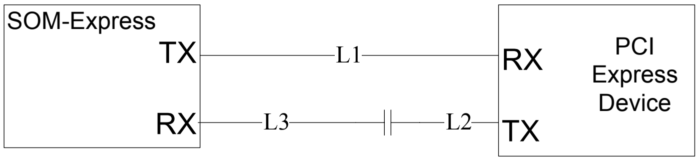


Figure 5-49 Topology #1 – SOM Express to PCI Express Device Down

Table 5-28 SOM Express to PCI Express			
L1	**L2**	**L3**	**Capacitor Value**
Max = 14.75 inches	Min = 0.25 inches Max = 14.5 inches	Max = 14.75 inches – L2	75 nF to 200 nF, Tolerance = 20%, Package: recommended to use 0603, or use 0402 if necessary

5.10.3.4 PCI Express Topology #2 and #3 – Device Down Routing

Both the ExpressCard and the docking topologies allow a maximum of 10 inches from SOM-Express pin to the pin of the down device. This maximum length takes into account all routing, including the breakout region, which should not exceed 0.25 inches per device. The TX and RX pairs must be routed interleaved, such that the pairs alternate between TX and RX on the carrier board to reduce crosstalk for microstrip and stripline topologies.

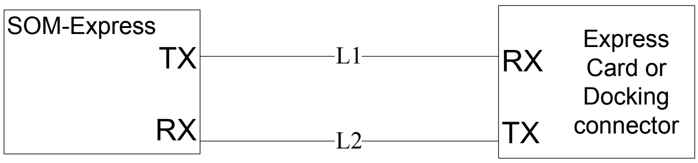


Figure 5-50 Topology #2 and #3 – SOM Express to Express Card or Docking Conn.

Table 5-29 SOM Express to Express Card		
L1	**L2**	**Capacitor Value**
Max = 10 inches	Max = 10 inches	75 nF to 200 nF, Tolerance = 20%, Package: recommend to use 0603, or use 0402 if necessary

5.11 Serial ATA

SOM-Express provides up to four Serial ATA (SATA) interface.

5.11.1 Signal Description

Table 5-30 shows SOM-Express Serial ATA signals for general purpose, including pin number, signals, I/0, and descriptions.

Table 5-30 Serial ATA Signal Description

Pin	Signal	I/O	Description
A16 A17	SATA0_TX+ SATA0_TX-	O	Serial ATA or SAS Channel 0 transmit differential pair
A19 A20	SATA0_RX+ SATA0_RX-	I	Serial ATA or SAS Channel 0 receive differential pair
B16 B17	SATA1_TX+ SATA1_TX-	O	Serial ATA or SAS Channel 1 transmit differential pair
B19 B20	SATA1_RX+ SATA1_RX-	I	Serial ATA or SAS Channel 1 receive differential pair
A22 A23	SATA2_TX+ SATA2_TX-	O	Serial ATA or SAS Channel 2 transmit differential pair
A25 A26	SATA2_RX+ SATA2_RX-	I	Serial ATA or SAS Channel 2 receive differential pair
B22 B23	SATA3_TX+ SATA3_TX-	O	Serial ATA or SAS Channel 3 transmit differential pair
B25 B26	SATA3_RX+ SATA3_RX-	I	Serial ATA or SAS Channel 3 receive differential pair
A28	ATA_ACT#	O	ATA (parallel and serial) or SAS activity indicator, active low

5.11.2 Design Guidelines

5.11.2.1 Serial ATA AC Coupling Requirements

Both the TX and RX SATA differential pairs require AC coupling capacitors. Figure 5-51 shows the connection for SOM-Express SATA signals. All AC coupling capacitors close to the transmitter (TX) and receiver (RX) are placed on the SOM-Express board. Please do not the place AC coupling capacitors on your carrier board.

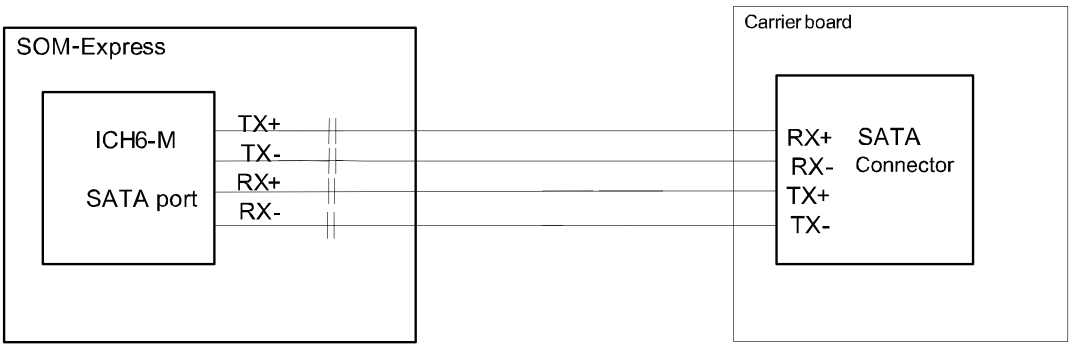


Figure 5-51 SATA interconnect example

5.11.2.2 Indicated LED Implementation

SOM-Express provides a signal (ATA_ACT#) to indicate SATA activity. In order for this signal to work in conjunction with Parallel ATA hard drives, it is recommended that designers implement glue logic. An example is shown in the Figure 5-52.
When low, ATA_ACT# indicates SATA device activity and should activate the Hard Drive LED. When tri-stated, the signal will not activate the LED. The Hard Drive LED is active low. An external pull-up to Vcc3_3 on ATA_ACT# is required if implemented.

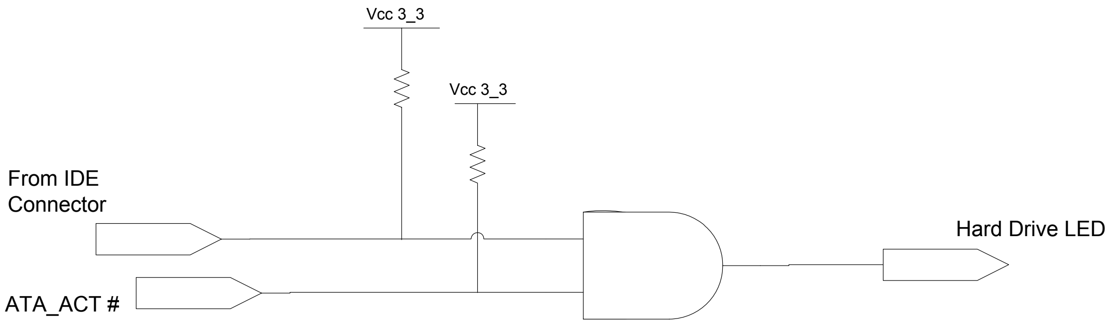


Figure 5-52 ATA_ACT# Circuit Example

5.11.2.3 Terminating Unused SATA interface Ports

If one of the SATA interface is not implemented, the unused port's TX and RX signals may be left unconnected on the carrier board.

5.11.3 Layout Guidelines

5.11.3.1 General routing and placement

- SATA signals must be ground referenced.
- Route all traces over continuous GND planes, with no interruptions. Avoid crossing over anti-etched areas if at all possible. Any discontinuity or split in the ground plane can cause signal reflections and should be avoid.
- Minimize layer changes. Use as few vias per SATA trace as possible (via count should include through hole connectors as an effective via). If a layer change is necessary, ensure that trace matching for either the TX or RX pair occurs within the same layer.
- Do not route SATA traces under crystals, oscillators, clock synthesizers, magnetic devices or ICs that use and/or duplicate clocks.
- Avoid stubs whenever possible. Utilize vias and connector pads as test points instead.
- In SOM-Express platforms, the SATA differential trace impendence target is 100 Ω ± 20%. Use an impedance calculator to determine the trace width and spacing required for the specific board stack-up being used, keeping in mind that the target is a 100 Ω ± 20%. Please refer to chapter 4 to get more information.

5.11.3.2 Serial ATA Trace length

- The length of the SATA differential pairs should be designed as short as possible. For direct-connected topology where the SATA differential signal pair is routed directly to a mobile SATA connector, we recommend the trace length be 9.5 inches for microstrip routing and 7 inches for stripline routing.

- The SATA differential pair trace should be trace length matched. The difference of two line traces in a TX or RX differential pair should be restricted to less than 20 mils, but even less trace mismatch is encouraged.

Figure 5-53 shows an example of SATA trace length pair matching. L_A must equal to L_A', L_B must equal to L_B', …and so on. We recommend minimizing layer change, ensuring that the differential pairs are equal if necessary.

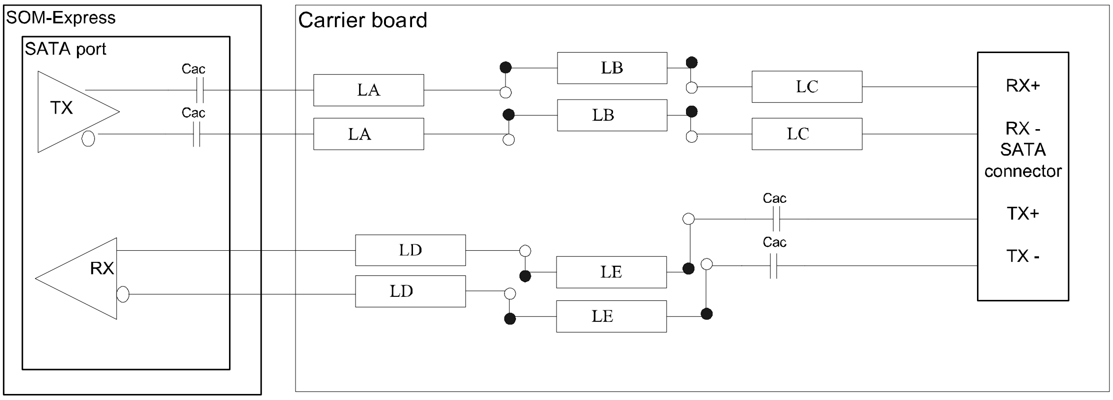


Figure 5-53 Example of SATA trace length pair matching

5.12 LPC

SOM-Express provides a LPC interface to some devices like Super I/O , FWH and others.

5.12.1 Signal Description

Table 5-32 shows SOM-Express LPC signals, including pin number, signals, I/0 and descriptions.

Table 5-32 LPC signals description

Pin	Signal	I/O	Description
B4,5,6,7	LPC_AD[0:3]	O	LPC multiplexed address, command and data bus
B3	LPC_FRAME#	O	LPC frame indicates the start of an LPC cycle
B8,B9	LPC_DRQ[0:1]#	O	LPC serial DMA request
A50	LPC_SERIRQ	O	LPC series interrupt
B10	LPC_CLK	O	LPC clock output – 33MHz nominal

5.12.2 Design Guidelines

5.12.2.1 LPC Design Considerations

Routing requirements for the TPM's LPC are as follows:

LPC_AD[0:3] are shared with the Firmware Hub (FWH) component and the Super I/O (SIO) device.
LPC_CLK should be connected to a 33 MHz clock.
LPC_FRAME# (cycle termination) is shared with FWH and the SIO.
LPC_SERIRQ (serialized IRQ) is shared with the SIO.

5.12.2.2 Signal Pull-Up Requirements

The LPC_AD [0:3] signals require pull-up resistors to maintain their state during the turnaround (TAR) periods of a cycle.
The LPC_DRQ [0:1] signals require pull-ups if they are not connected to a LPC peripheral device. This will keep them in the inactive state.
See Table 5-33 below for recommended pull-up values. Some host devices will incorporate these pull-ups internally. Other signals may or may not require pull-up resistors, depending on the specific system implementation.

Table 5-33 Recommended Pull-Up Values

Signal Name	Pull-Up
LAD[3:0]	15k - 100k Ω
LDRQ[1:0]#	15k - 100k Ω

5.12.3 Layout Guidelines

5.12.3.1 Placement considerations

Optimum routing can typically be achieved by placing the TPM in proximity to other LPC peripherals (e.g., firmware hub, super I/O).
The TPM is a security device that should be shielded as much as possible from physical access. In high-security implementations, a number of mechanisms can be utilized to detect or prevent physical system intrusion, but such mechanisms are beyond the scope of this design guide.

5.12.4 Application Notes

Some signals from the Super I/O, like Serial port, Parallel port, Floppy, IR, KBC, etc., can connect to SOM-Express via the LPC Bus. Figure 5-54 shows the architecture of the LPC interface. We will make some examples. You can get more information in the Super I/O data sheet.

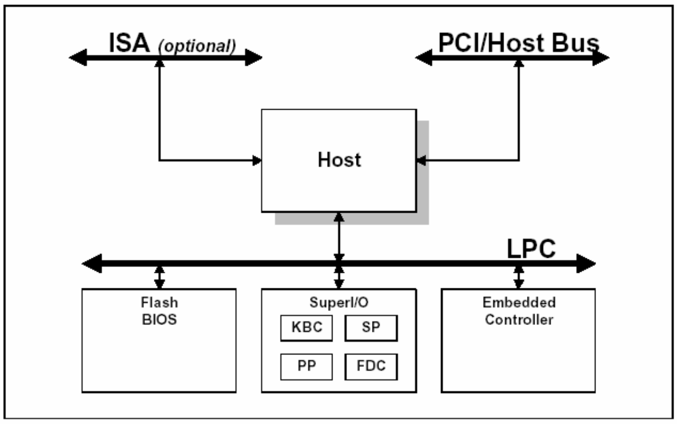


Figure 5-54 Architecture of LPC interface

5.12.4.1 Serial port

Sometimes, in order to avoid EMI issues, we often separate ground to frame ground (I/O ground). Adding beads and capacitors to the carrier board is necessary. Figure 5-55 shows the Serial Bus Connection.

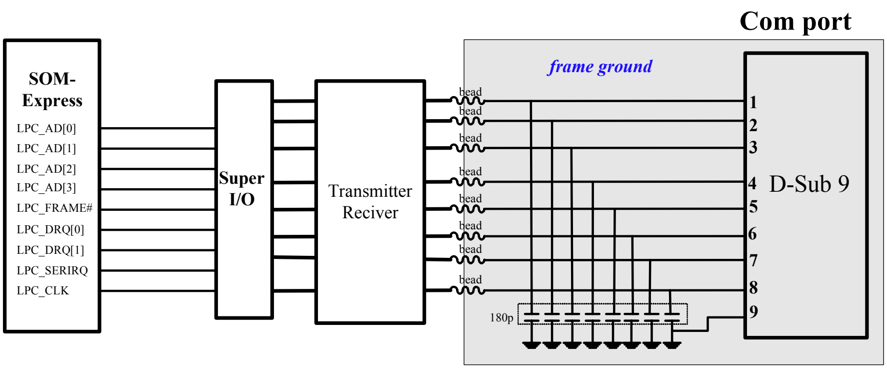


Figure 5-55 Serial Bus Connection

5.12.4.2 PS/2 Keyboard and Mouse

For a general design concept, the keyboard and mouse should be far away from audio and VGA signal traces to avoid crosstalk. According to general keyboard and mouse power specifications, the traces of keyboard and mouse power trace should be routed to afford 1A. The power can be sourced from the system power plane through a ferrite bead and then a fuse. A capacitor should be added behind, with the ground of the capacitor place at the keyboard/mouse ground. A practical schematic is shown in figure 5-56.

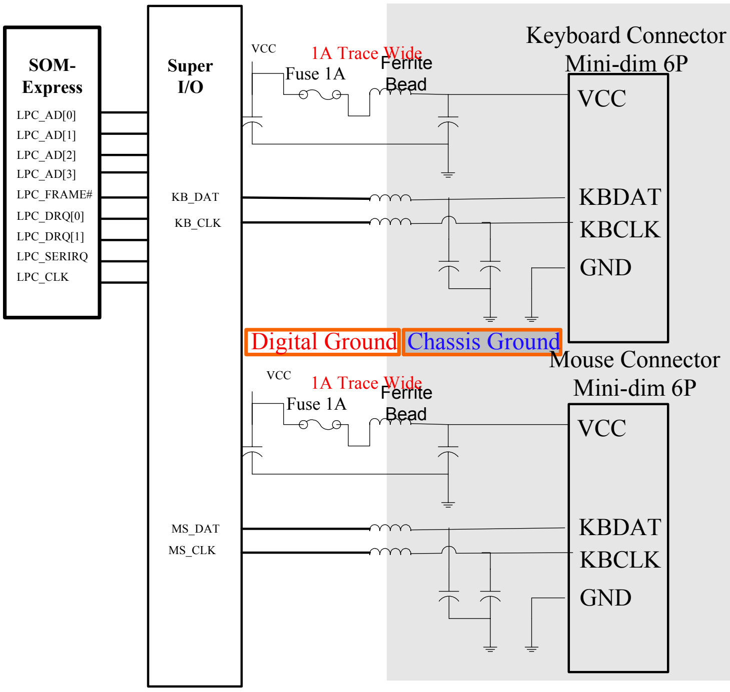


Figure 5-56 Keyboard and Mouse connection

To avoid EMI and ESD, the ground plane of the keyboard/mouse connector and other digital ground planes, should be separated with an isolation moat (which is recommended to be at least 40 mils) to the power planes. Digital ground and chassis ground should be connected via screw holes to assure the integrity of the ground plane.

5.12.4.3 LPT/Floppy

5.12.4.4 EMI Considerations

I/Os like LPT ports/Floppy and COM ports, should be physically isolated from digital circuitry, analog circuitry, and power and ground planes. This isolation prevents noise sources located elsewhere on the PCB from corrupting susceptible circuits. An example is power plane noise from digital circuits entering the power pins of analog devices, audio components, I/O filters and interconnects, and so on.
Each and every I/O port (or section) must have a partitioned ground/power plane. Lower frequency I/O ports may be bypassed with high-frequency capacitors located near the connectors.
Trace routing on the PCB must be controlled to avoid recouping RF currents into the cable shield. A clean ground must be located at the point where cables leave the system. Both power and ground planes must be treated equally, as these planes act as a path for RF return currents.
To implement a clean ground, use of a partition or moat is required. The clean area should be:

1. 100% isolated with I/O signals entering and exiting via an isolation transformer or an optical device.
2. Data line filtered; or
3. Filtered through a high-impedance common-mode inductor (choke) or protected by a ferrite bead-on-lead component.

5.12.4.5 ESD Protection

The PCB must incorporate protection against electrostatic discharge (ESD) events that might enter at I/O signal and electrical connection points. The goal is to prevent component or system failures due to externally sourced ESD impulses that may be propagated through both radiated and conducted mechanisms.
Several commonly used design techniques for ESD protection that may be implemented on a PC for high-level pulse suppression include the following:

1. High voltage capacitors. These disc-ceramic capacitors must be rated at 1500 V (1 KV) minimum. Lower-voltage capacitors may be damaged by the first occurrence of an ESD pulse. This capacitor must be located immediately adjacent to the I/O connector.
2. TVS components. These are semiconductor devices specifically designed for transient voltage suppression applications. They have the advantage of a stable and fast time constant to avalanche, and a stable clamping level after avalanche.
3. LC filters. An LC filter is a combination of an inductor and a capacitor to ground. This constitutes a low-pass LC filter that prevents high-frequency ESD energy from entering the system. The inductor presents a high-impedance source to the pulse, thus attenuating the impulse energy that enters the system. The capacitor, located on the input side of the inductor will shunt high-frequency ESD spectral level components to ground. An additional benefit of this circuit combination is enhancement of radiated EMI noise suppression.

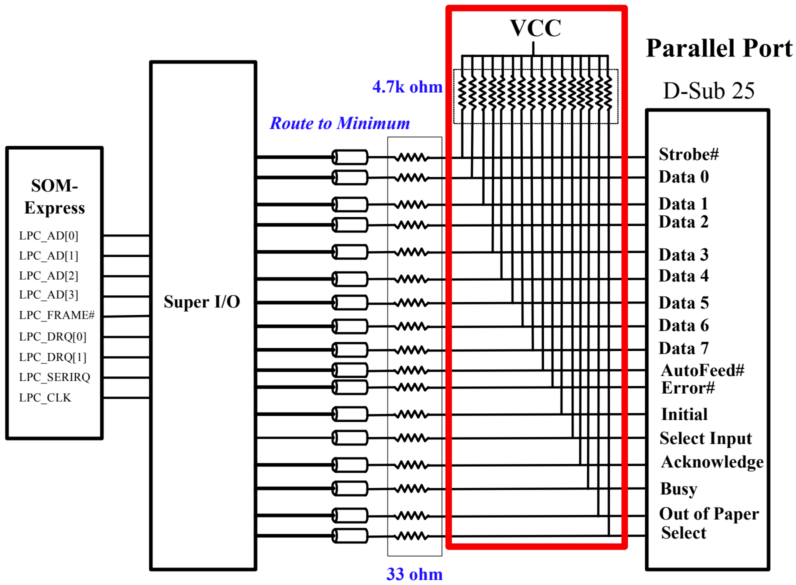


Figure 5-57 LPT Connection

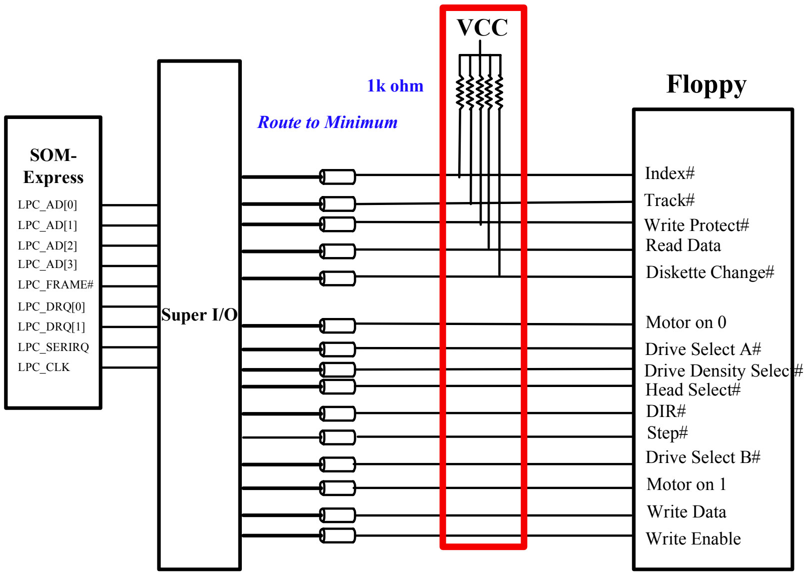


Figure 5-58 Floppy Connection

Chapter 6 Power Delivery Guidelines

This chapter provides the power consumption guidelines for SOM-Express modules and the ATX/AT power supply design recommendations for customer's reference.

6.1 SOM-Express Power Consumption

The power consumption of each SOM-Express module is shown below. The power consumption for different SOM-Express module power requirements will be necessary.

Table 6.1 SOM-5780 Power Consumption			
SOM-5780 A1013 CPU : CPU760 2.0GHz, Memory : Transcend DDRII 533 1GB			
	+5VSB(A)	+12V(A)	Watts
BIOS(1 min)	0.31	2.42	30.59
XP IDLE (1 min)	0.31	1.81	23.27
XP Standby(S1)(1 min)	0.31	1.11	14.87
XP Standby(S3)(1 min)	0.41	0	2.05
XP Run HCT- 11.2 (10 min)	0.31	2.62	32.99
5VSB power	0.4	0	2

SOM-5780 A1013 CPU : CPU745 1.8GHz, Memory : Transcend DDRII 533 1GB			
	+5VSB(A)	+12V(A)	Watts
BIOS(1 min)	0.3	2.22	28.14
XP IDLE (1 min)	0.3	1.6	20.7
XP Standby(S1)(1 min)	0.29	1.03	13.81
XP Standby(S3)(1 min)	0.41	0	2.05
XP Run HCT- 11.2 (10 min)	0.31	2.38	30.11
5VSB power	0.38	0	1.9

SOM-5780 A1013 CPU : CPU738 1.4GHz, Memory : Transcend DDRII 533 1GB			
	+5VSB(A)	+12V(A)	Watts
BIOS(1 min)	0.28	1.62	20.84
XP IDLE (1 min)	0.28	1.33	17.36
XP Standby(S1)(1 min)	0.28	1.06	14.12
XP Standby(S3)(1 min)	0.39	0	1.95
XP Run HCT- 11.2 (10 min)	0.28	1.75	22.4
5VSB power	0.36	0	1.8

SOM-5780 A1013 CPU : CPU373 1.0GHz, Memory : Transcend DDRII 533 1GB			
	+5VSB(A)	+12V(A)	Watts
BIOS(1 min)	0.33	1.5	19.65
XP IDLE (1 min)	0.32	1.25	16.6
XP Standby(S1)(1 min)	0.32	1.07	14.44
XP Standby(S3)(1 min)	0.43	0	2.15
XP Run HCT- 11.2 (10 min)	0.31	1.49	19.43
5VSB power	0.42	0	2.1

Table 6.2 SOM-5782 Power Consumption

SOM-5782 A1011 CPU : CPU T2500 2.0GHz Memory : Transcend DDRII 667 1GB			
	+V5SB(A)	+V12(A)	Watt
BIOS(1 min)	0.26	2.02	25.54
XP IDLE (1 min)	0.26	1.58	20.26
XP Standby(S1)(1 min)	0.24	1.43	18.36
XP Standby(S3)(1 min)	0.39	0	1.95
XP Run HCT- 11.2 (10 min)	0.25	2.1	26.45
5VSB power	0.29	0	1.45

SOM-5782 A1011 CPU : CPU L2400 1.66GHz Memory : Transcend DDRII 667 1GB			
	+V5SB(A)	+V12(A)	Watt
BIOS(1 min)	0.22	1.45	18.5
XP IDLE (1 min)	0.23	1.13	14.71
XP Standby(S1)(1 min)	0.24	0.95	12.6
XP Standby(S3)(1 min)	0.37	0	1.85
XP Run HCT- 11.2 (10 min)	0.29	1.58	20.41
5VSB power	0.24	0	1.2

SOM-5782 A1011 CPU : CPU 423 1.06GHz Memory : Transcend DDRII 667 1GB			
	+V5SB(A)	+V12(A)	Watt
BIOS(1 min)	0.24	1.22	15.84
XP IDLE (1 min)	0.23	1.03	13.51
XP Standby(S1)(1 min)	0.21	0.89	11.73
XP Standby(S3)(1 min)	0.32	0	1.6
XP Run HCT- 11.2 (10 min)	0.24	1.26	16.32

5VSB power	0.24	0	1.2

SOM-5782 A1011 CPU : CPU T2600 2.16GHz Memory : Transcend DDRII 667 1GB			
	+V5SB(A)	+V12(A)	Watt
BIOS(1 min)	0.24	2.02	25.44
XP IDLE (1 min)	0.25	1.57	20.09
XP Standby(S1)(1 min)	0.22	1.4	17.9
XP Standby(S3)(1 min)	0.39	0	1.95
XP Run HCT- 11.2 (10 min)	0.29	2.11	26.77
5VSB power	0.24	0	1.2

Notes:

1. Operates entirely from 12 Volt input power.
2. To accommodate future modules, it is recommended that the 12 V supply be capable of delivering 5 amperes average current to the SOM-Express module (with momentary peak current up to 7.5 amperes).
3. It is also recommended that the thermal management solution is capable of removing 40 watts from the SOM-Express module's heat spreader plate while maintaining conservative operating temperatures.

6.2 Design Guidelines

6.2.1 ATX Power Delivery Block Diagram

An ATX power source will provide 12 V , -12 V , 5 V , -5 V , 3.3 V , 5 VSBY power , if other voltage is required (3.3 VSBY , LAN 2.5….) on the carrier board, an additional switching regulator or LDO will be necessary.

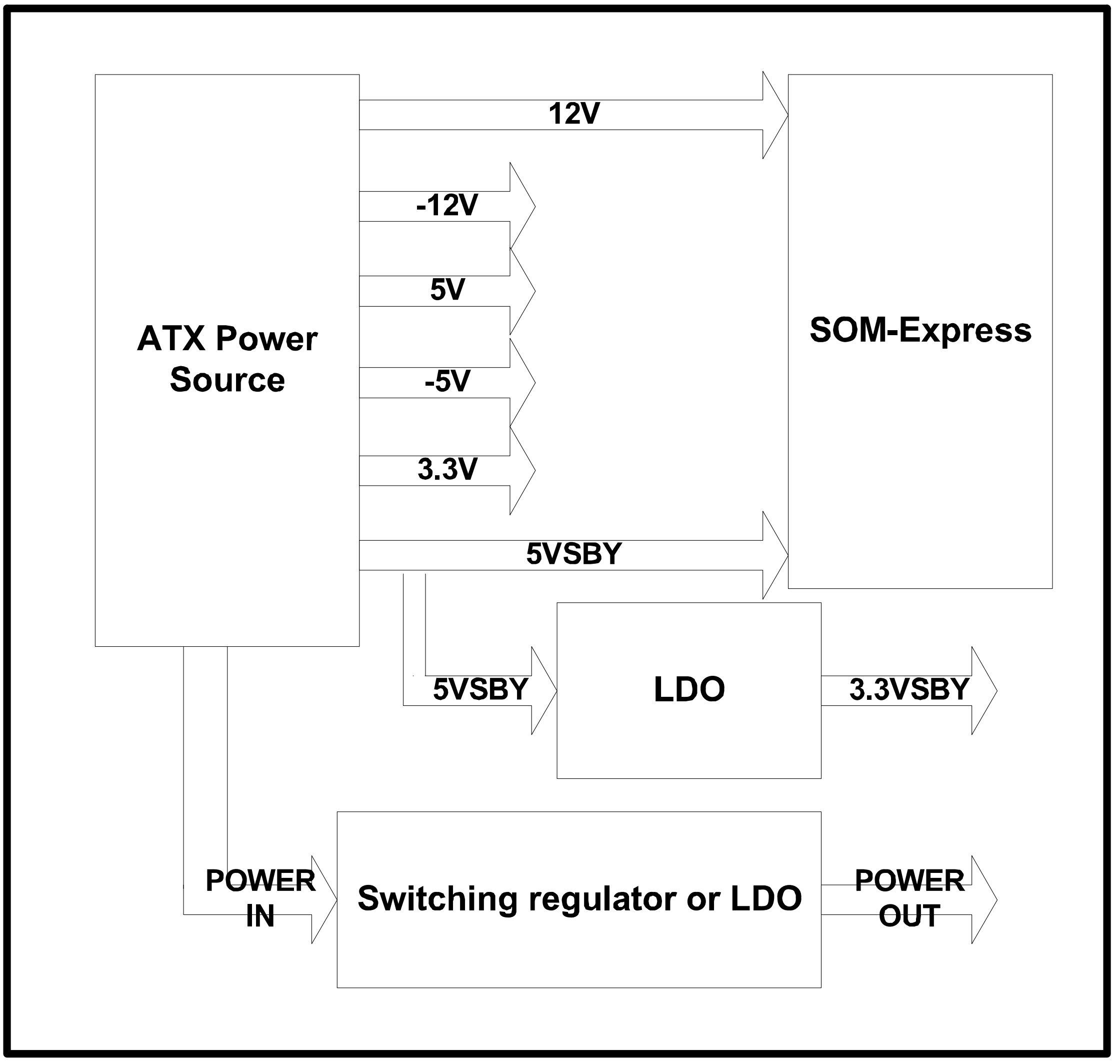


Figure 6-1 ATX Power Delivery Block Diagram

6.2.2 AT Power Delivery Block Diagram

An AT power source will provide 12 V and 5 V power. An additional switching regulator or LDO will be required to simulate the ATX power (3.3 V…) .There will be no standby voltage when an AT power source is used.

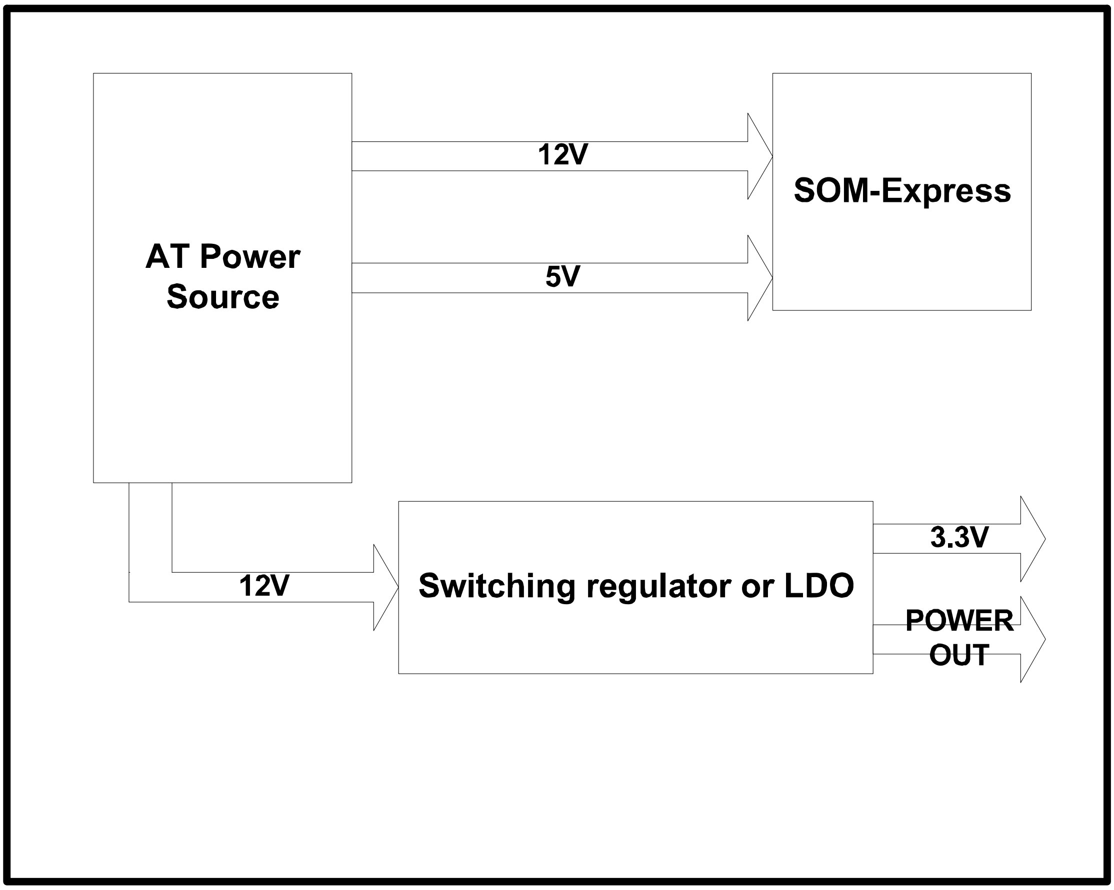


Figure 6-2 AT Power Delivery Block Diagram

Chapter 7 Carrier Board Mechanical Design Guidelines

7.1 SOM-Express Mechanical Dimensions

The PCB size of the SOM-Express module is 125mm x 95mm, COM Express Basic Module. The PCB thickness may be 2mm to allow high layer count stack-ups and facilitate a standard 'z' dimension between the Carrier Board and the top of the heat-spreader.

The holes shown in this drawing are intended for mounting the module / heat-spreader combination to the Carrier Board. An independent, implementation specific set of holes and spacers shall be used to attach the heat-spreader to the module. Figure 7-1 shows the SOM-Express module board mechanical dimensions. The unit is millimeter.

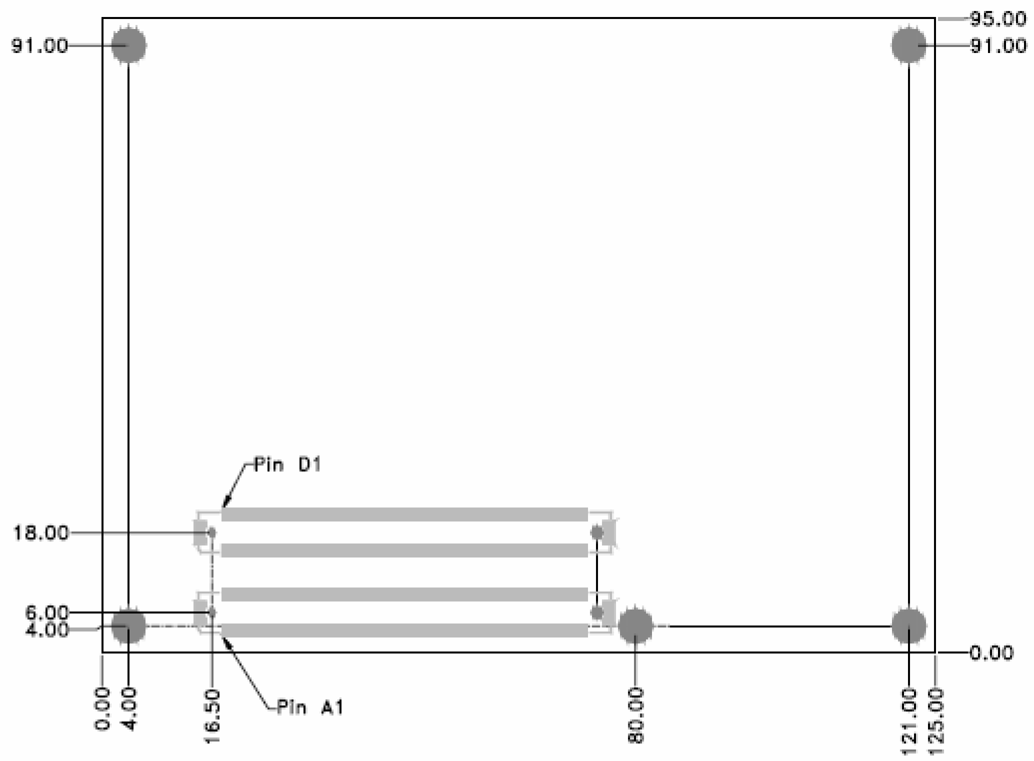


Figure 7-1: SOM-Express Module Board Mechanical Dimensions

Tolerances shall be ± 0.25mm [±0.010"], unless noted otherwise. The tolerances on the module connector locating peg holes (dimensions [15.50, 6.00] and [16.50, 18.00]) shall be ± 0.10mm [±0.004"].
The 440 pin connector pair shall be mounted on the backside of the PCB and is seen "through" the board in this view.
The 5 mounting holes shown shall use 6mm diameter pads and shall have 2.7mm plated holes, for use with 2.5mm hardware. The pads shall be tied to the PCB ground plane.

7.2 SOM Express Module Connector

The module connector for Pin-out Type 2 shall be a 440-pin receptacle that is composed of 2 pieces of a 220-pin, 0.5 mm pitch receptacle. The pair of connectors may be held together by a plastic carrier during assembly to allow handling by automated assembly equipment. The connectors shall be qualified for LVDS operation up to 6.25GHz, to support PCI Express Generation 2 signaling speeds. Sources for the individual 220-piin receptacle are AMP / Tyco 3-1318490-6 0.5mm pitch Free Height 220 pin 4H Receptacle, or equivalent AMP / Tyco 8-1318490-6 0.5mm pitch Free Height 220 pin 4H Receptacle, or equivalent (same as previous part, but with anti-wicking solution applied). A source for the combined 440-pin receptacle (composed of 2 pieces of the 220 pin receptacle held by a carrier) is: AMP / Tyco 3-1827231-6 with 0.5mm pitch Free Height 440 pin 4H Receptacle or equivalent.

Note: the part number above shown with a leading '8' has an anti-wicking solution applied that may help in processing with an aggressive flux. The other versions of the parts may also be made available with this solution by the vendor. The module connector is a receptacle by virtue of the vendor's technical definition of a receptacle, and to some users it looks like a plug.

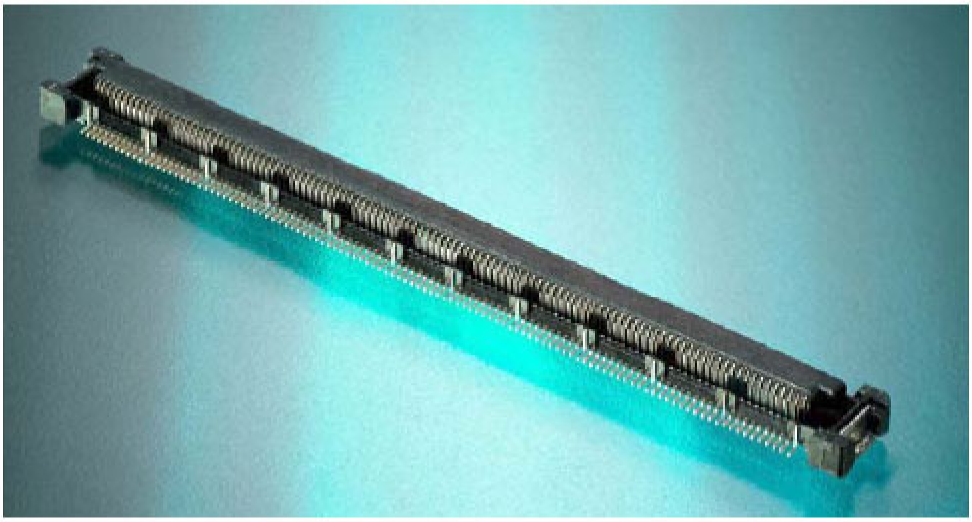


Figure 7-2: SOM-Express Module Receptacle

7.3 SOM Express Carrier Board Connector

The Carrier Board connector for module Pin-out Type 2 shall be a 440-pin plug that is composed of 2 pieces of a 220-pin, 0.5 mm pitch plug. The pair of connectors may be held together by a plastic carrier during assembly to allow handling by automated assembly equipment. The connectors shall be qualified for LVDS operation up to 6.25GHz, to support PCI Express Generation 2 signaling speeds. The Carrier Board plugs are available in a variety of heights. The Carrier Board shall use either the 5 mm or 8 mm heights.

A source for the individual 5mm stack height 220-piin plug is AMP / Tyco 3-1327253-6 0.5mm pitch Free Height 220 pin 5H Plug, or equivalent

A source for the combined 5mm stack height 440-pin plug (composed of 2 pieces of the 220 pin plug held by a carrier) is: AMP / Tyco 3-1827233-6 0.5mm pitch Free Height 440 pin 5H Plug, or equivalent

A source for the individual 8mm stack height 220-piin plug is AMP / Tyco 3-1318491-6 0.5mm pitch Free Height 220 pin 8H Plug, or equivalent, AMP / Tyco 8-1318491-6 0.5mm pitch Free Height 220 pin 8H Plug, or equivalent (same as previous part, but with anti-wicking solution applied)
A source for the combined 8mm stack height 440-pin plug (composed of 2 pieces of the 220 pin plug held by a carrier) is: AMP / Tyco 3-5353652-6 0.5mm pitch Free Height 440 pin 8H Plug, or equivalent.

Note: the part number above shown with a leading ‘8’ has an anti-wicking solution applied that may help in processing with an aggressive flux. The other versions of the parts may also be made available with this solution by the vendor. The Carrier Board connector is a plug by virtue of the vendor’s technical definition of a plug, and to some users it looks like a receptacle.

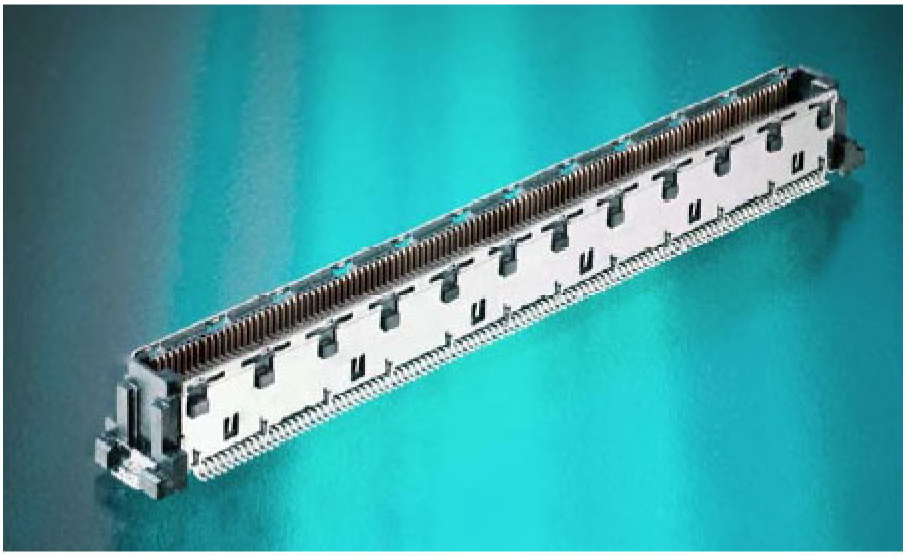
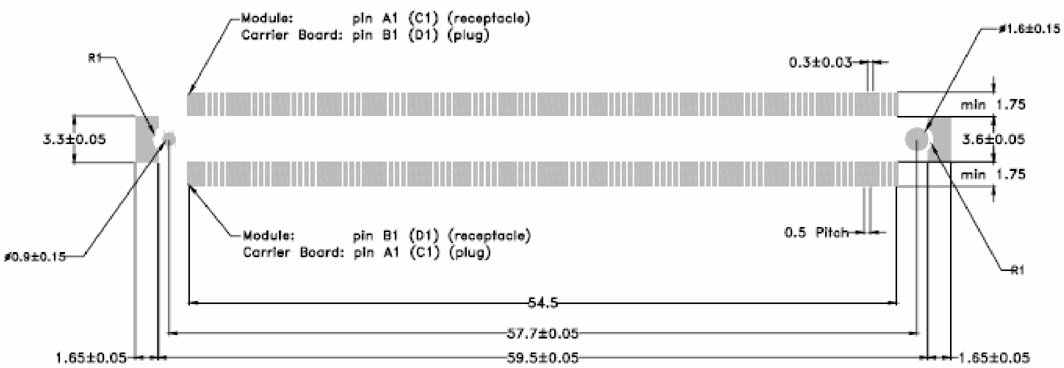


Figure 7-3: SOM-Express Carrier Board Plug (8mm Version)

7.4 SOM Express Connector PCB Pattern



All dimensions in mm.

Figure 7-4: SOM-Express Connector PCB Pattern

7.5 SOM Express Module Connector Pin Numbering

Pin numbering for 440-pin module receptacle. This is a top view of the receptacle, looking into the receptacle, as mounted on the backside of the module.

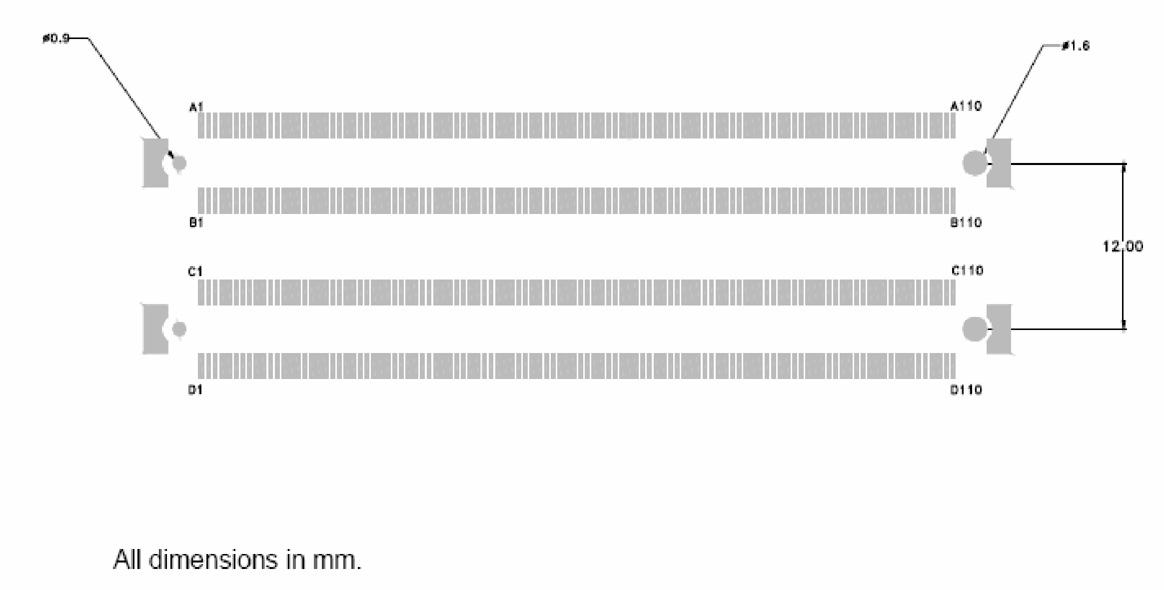


Figure 7-5: SOM-Express Module Connector Pin Numbering

7.6 SOM-Express Carrier Board Connector Pin Numbering

Pin numbering for 440-pin carrier-board plug. This is a top view, looking into the plug as mounted on the Carrier Board.

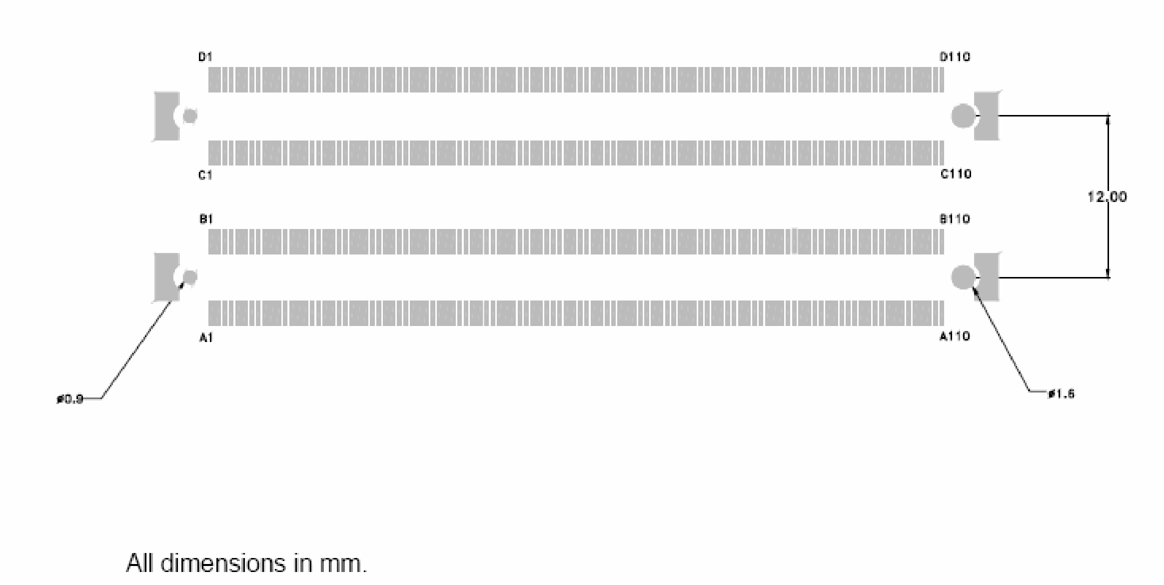


Figure 7-6: SOM-Express Carrier Board Connector Pin Numbering

Chapter 8 Heatsink Recommended Design

8.1 Material of Heatsink

The thermal conductivity of the heatsink's material has a major impact on cooling performance. Thermal conductivity is measured in W/mK; higher values mean better conductivity.
As a rule of thumb, materials with a high electrical conductivity also have a high thermal conductivity.
The following materials are commonly used for heatsinks:

Aluminium. It has a thermal conductivity of 205W/mK, which is good (as a comparison: steel has about 50W/mK). The production of aluminium heatsinks is inexpensive; they can be made using extrusion Due to its softness, aluminium can also be milled quickly; die-casting and even cold forging are also possible. Aluminium is also very light (thus, an aluminium heatsink will put less stress on its mounting when the unit is moved around).

Copper. Copper's thermal conductivity is about twice as high as aluminium - almost 400W/mK. This makes it an excellent material for heatsinks; but its disadvantages include high weight, high price, and less choice as far as production methods are concerned. Copper heatsinks can be milled, die-cast, or made of copper plates bonded together; extrusion is not possible.

Combination of Aluminium and Copper. To combine the advantages of aluminium and copper, heatsinks can be made of aluminium and copper bonded together. Here, the area in contact with the heat source is made of copper, which helps lead the heat away to the outer parts of the heatsink. Keep in mind that a copper embedding is only useful if it is tightly bonded to the aluminium part for good thermal transfer. This is not always the case, especially not with inexpensive coolers. If the thermal transfer between the copper and the aluminium is poor, the copper embedding may do more harm than good.

Silver. Silver has an even higher thermal conductivity than copper, but only by about 10%. This does not justify the much higher price for heatsink production - however, pulverized silver is a common ingredient in high-end thermal compounds

Alloys. Alloys have lower thermal conductivity than pure metals, but may have better mechanical or chemical (corrosion) properties.

8.2 Thermal Interface Material

It is important to understand and consider the impact the interface between the processor and heatsink base has on the overall thermal solution. Specifically, the bond line thickness, interface material area, and interface material thermal conductivity must be selected to optimize the thermal solution. It is important to minimize the thickness of the thermal interface material, commonly referred to as the bond line thickness. A large gap between the heatsink base and processor die yields a greater thermal resistance. The thickness of the gap is determined by the flatness of both the heatsink base and the die, plus the thickness of the thermal interface material (i.e., thermal grease), and the clamping force applied by the heatsink attachment method. To ensure proper and consistent thermal performance, the thermal interface material (TIM) and application process must be properly designed.

Alternative material can be used at the users' discretion. The entire heatsink assembly, including the heatsink, attach method, and thermal interface material, must be validated together for specific applications.

8.3 Attachment Method of Thermal Solution

The thermal solution can be attached to the motherboard in a number of ways. The thermal solutions have been designed with mounting holes in the heatsink base. A plastic rivet is currently in development that can be used to fasten smaller heatsinks. For larger and heavier heatsinks, a fastening system consisting of screws, springs, and secured with a nut should be used. The entire heatsink assembly must be validated together for specific applications, including the heatsink, attach method, and thermal interface material.

8.4 Grounding Issues

The mounting holes on all Advantech SOM-Express are connected to digital circuit ground (GND) for improved EMC performance. Using conductive screws and distance keepers will also connect the heat spreader and attached heat sink to GND. In some applications the heat sink or heat spreader will be directly screwed with the inner surface of the chassis. In some cases, however, it may not be desirable to have a direct connection of circuit ground (GND) and chassis ground through the heat sink and / or heat spreader. System designers should take this into account when defining system grounding.

8.5 Air intake clearance and Airflow of Heatsink

The heatsink were designed to maximize the available space within the volumetric keep-out zone. These heatsinks must be oriented in a specific direction relative to the processor keep-out zone and airflow. In order to use this design, the processor must be placed on the PCB in an orientation so the heatsink fins will be parallel to the airflow.

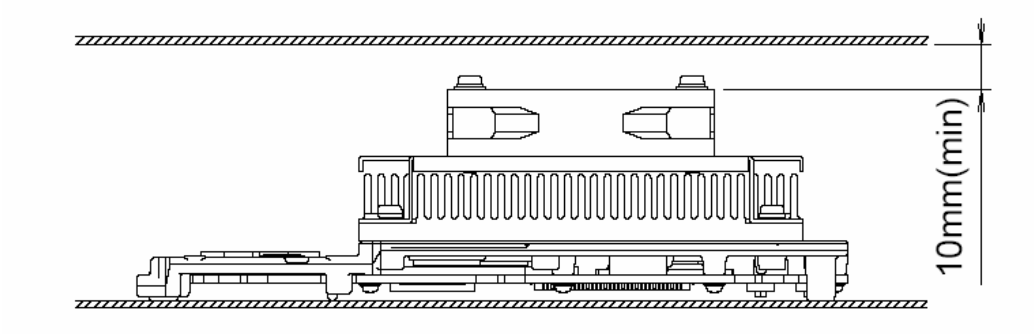


Figure 8-1: Air Intake Clearance

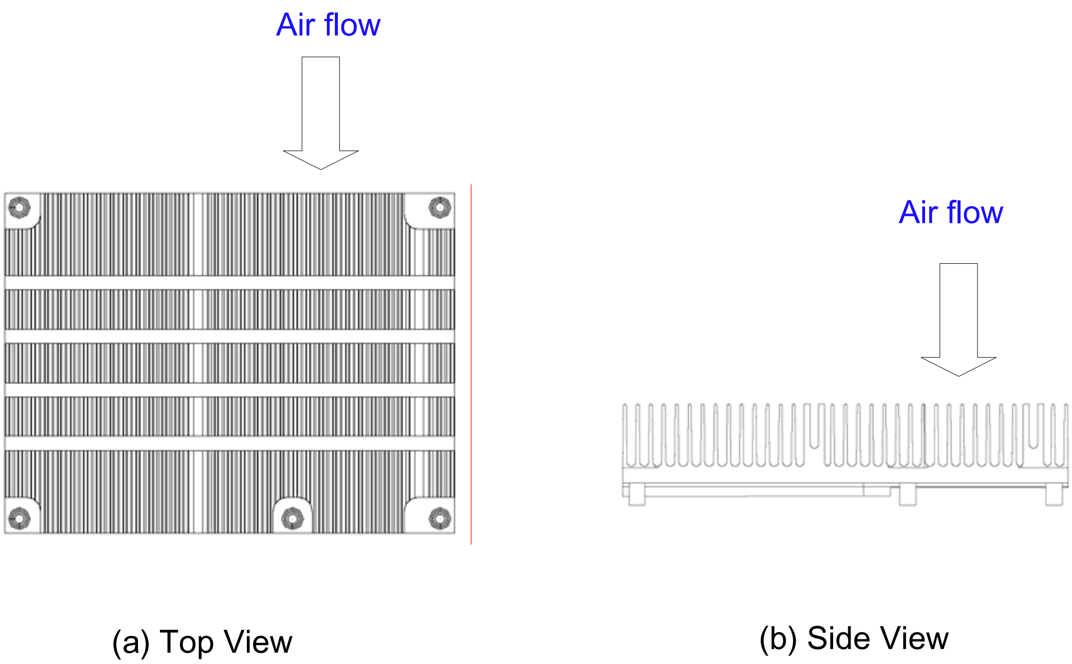


Figure 8-2: Air Flow Direction

8.6 SOM-Express Thermal solution Specification

Module should be equipped with a heat-spreader. This heat-spreader by itself does not constitute the complete thermal solution for a module but provides a common interface between modules and implementation-specific thermal solutions.
The overall module height from the bottom surface of the module board to the heat-spreader top surface shall be 13mm for SOM-Express modules. The module PCB and heat-spreader may be used which allows use of readily available standoffs.

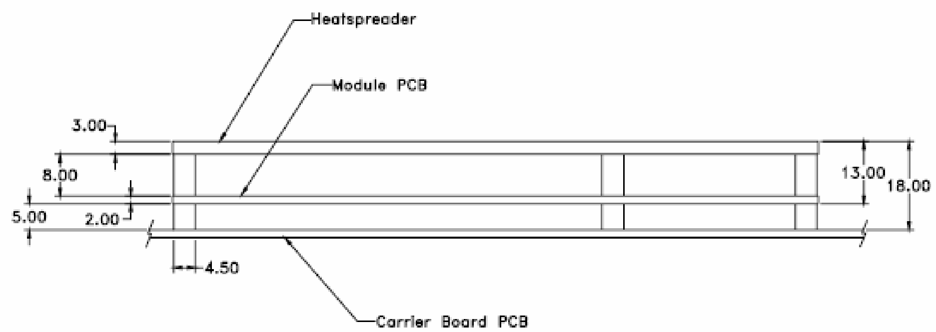
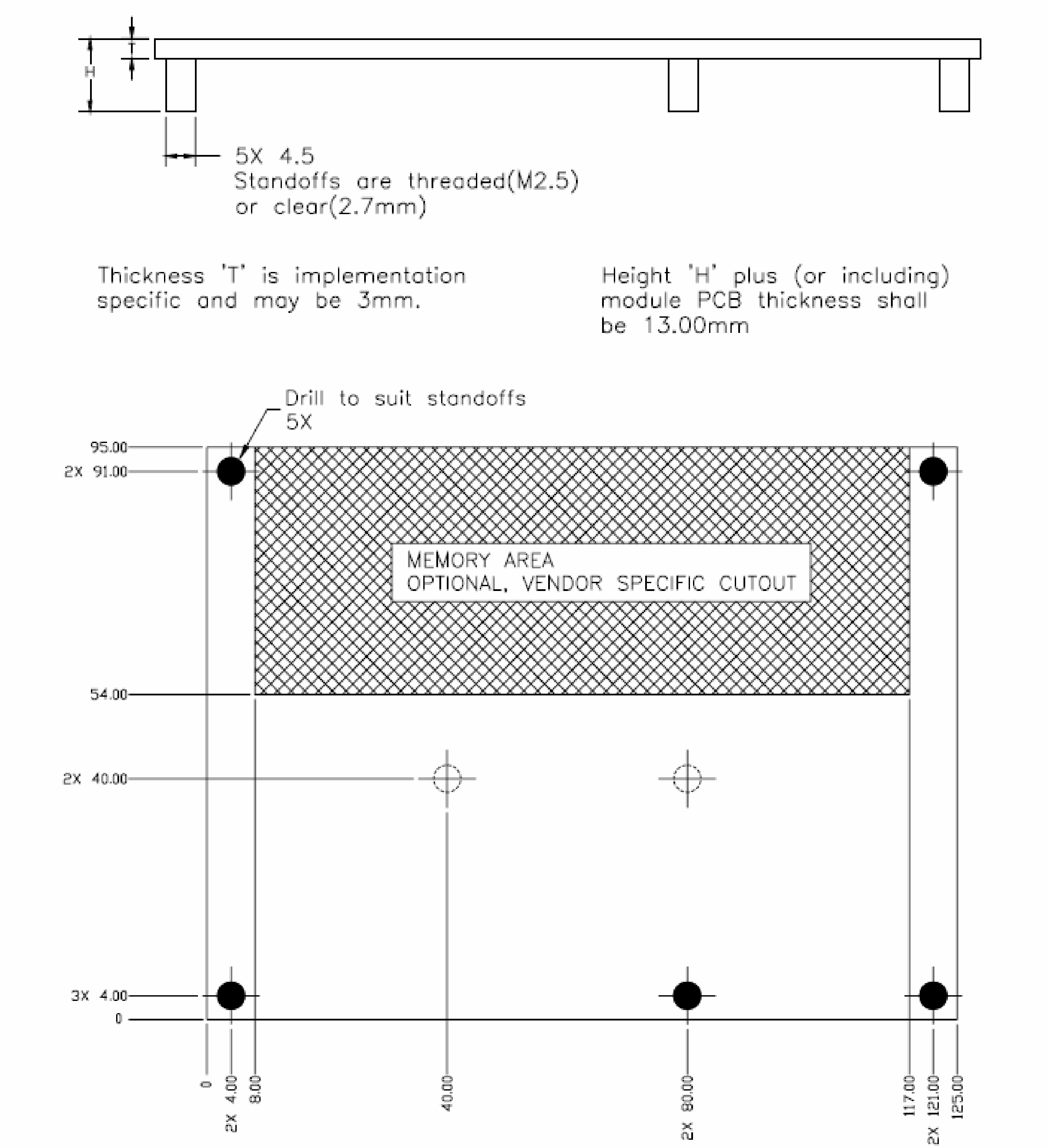


Figure 8-3: Overall Height for Heat-Spreader in SOM-Express Modules

Tolerances (unless otherwise specified):
Z (height) dimensions should be ±0.8mm [±0.031"] from top of Carrier Board to top of heat-spreader.
Heat-spreader surface should be flat within 0.2mm [.008"] after assembly.
Interface surface finish should have a maximum roughness average (Ra) of 1.6 μ m[63 μ in].
The critical dimension in Figure 8-3 is the module PCB bottom side to heat-spreader top side. This dimension shall be 13.00mm±0.65mm [±0.026"].
Figure 8-3 shows a cross section of a module and heat-spreader assembled to a Carrier Board using the 5mm stack height option. If 8mm Carrier Board connectors are used, the overall assembly height increases from 18.00mm to 21.00mm.



All dimensions are in mm. X-Y tolerances shall be ±0.3mm [±0.012"]

Figure 8-4: SOM-Express Module Heat-Spreader

The interior holes at coordinates (40, 40) and (80, 40) are tapped through holes with a M2.5 thread. The interior holes do not receive standoffs. These holes may be sealed on the module side by an adhesive backed foil, or they may be blind tapped holes with a minimum thread depth of 2.5mm. They are intended to allow additional attachment points to the heat-spreader from outside the module.

8.7 Component Height – Module Back and Carrier Board Top

Parts mounted on the backside of the module (in the space between the bottom surface of the module PCB and the Carrier Board) shall have a maximum height of 3.8mm (dimension 'B' in Figure 8-5)

With the 5mm stack option, the clearance between the Carrier Board and the bottom surface of the module's PCB is 5 mm (dimension 'A' in Figure 8-5). Using the 5mm stack option, components placed on the Carrier Board topside under the module envelope shall be limited to a maximum height of 1mm (dimension 'C' in Figure 8-5), with the exception of the mating connectors. Using Carrier Board topside components up to 1mm allows a gap of 0.2mm between Carrier Board module bottom side components. This may not be sufficient in some situations. IN Carrier Board applications in which vibration or board flex is a concern, then the Carrier Board component height should be restricted to a value less than 1mm that yields a clearance that is sufficient for the application.

If the Carrier Board uses the 8mm stack option (dimension 'A' in Figure 8-5), then the Carrier Board topside components within the module envelope shall be limited to a height of 4mm (dimension 'C' in Figure 8-5), with the exception of the mating connectors. Using Carrier Board topside components up to 4mm allows a gap of 0.2mm between Carrier Board topside components and module bottom side components. This may not be sufficient in some situation. IN Carrier Board applications in which vibration or board flex is a concern, then the Carrier Board component height should be restricted to a value less than 4mm that yields a clearance that is sufficient for the application.

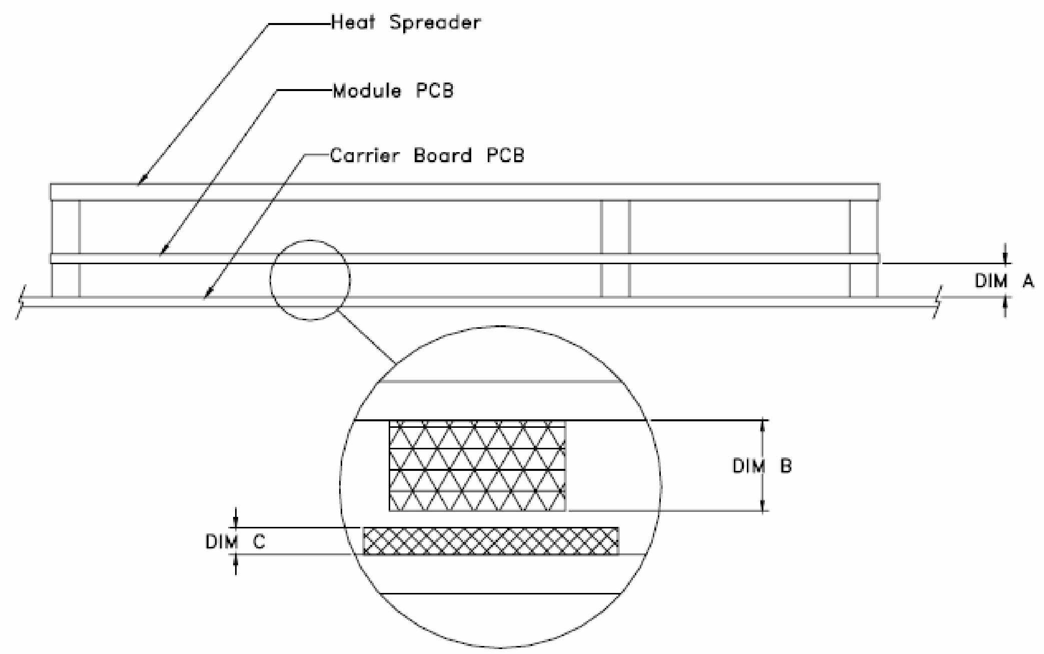


Figure 8-5: Component Clearances Underneath Module

8.8 Advantech Heatsink Information

8.8.1 Vendor List

Table 8.1: Vendor list	
Aluminum Extruded Heat-Spreader/Heat-Sink, Reference No. EID –BAN15-ALX-003SS and EID-LPT13-ALX-003	
CoolerMaster* Passive Heat-Spreader (includes heat-spreader, mounting clip, thermal interface material, retention mechanism, backplate, and five mounting screw) Active Heat-Sink (includes fan heat-sink, mounting clip, thermal interface material, retention mechanism, backplate, and five mounting screws) CoolerMaster* Part Number: ECC-00250-01-GP/ECC-00253-01-GP	
CoolerMaster 9F./ No. 786, Chung-Cheng Rd. Chung Ho City Taipei Hsien, Taiwan, R.O.C	Contact: Mike Chang Telephone: 886-2-3234-0050 ext.184 mike_chang@coolermater.com.tw
Thermal Interface Material	
Shin-Etsu Micro Si, Inc. 10028 S. 51stSt. Phoenix, AZ 85044	Contact: (480)893-8898 http://www.microsi.com

8.8.2 Heat-Spreader

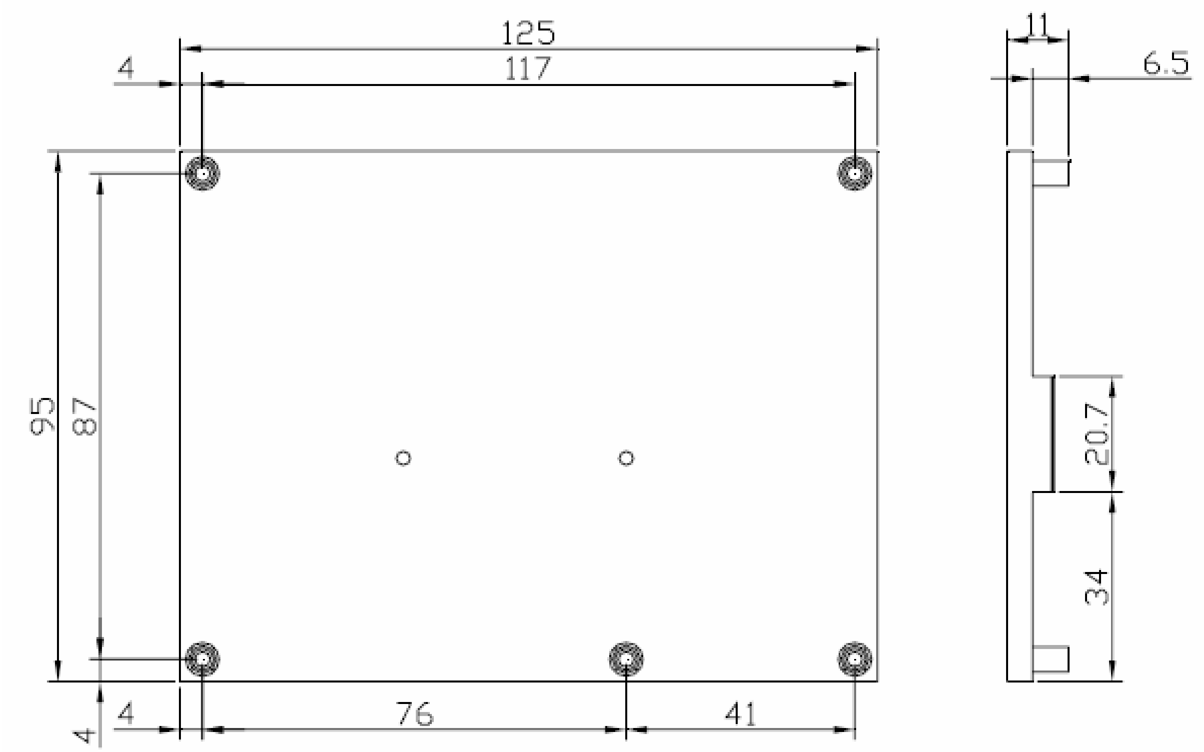
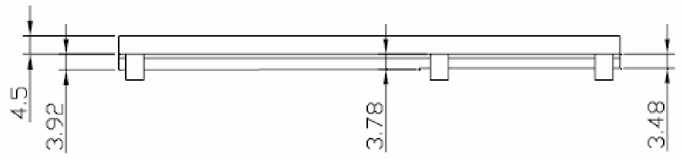


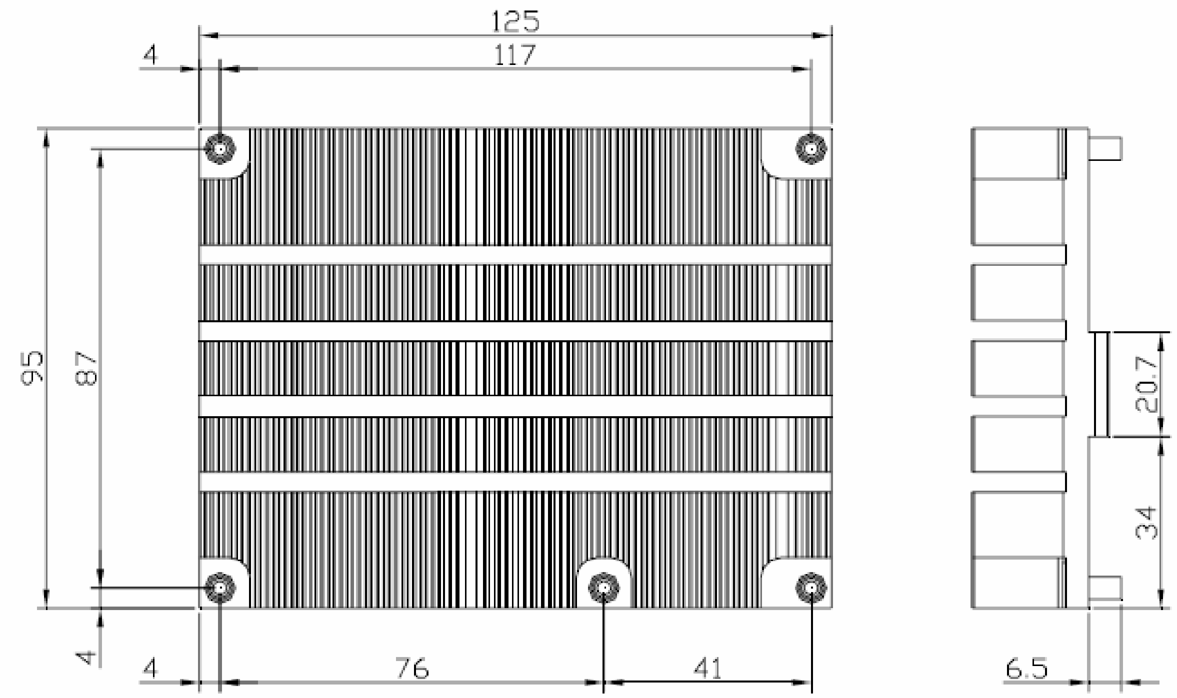
Figure 8-6: SOM-Express Heat-Spreader

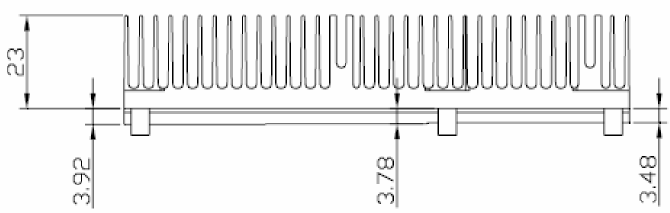


General Dimension Tolerances (Unit : mm)			
0	—	30	± 0.2
31	—	60	± 0.3
61	—	100	± 0.4
101	and	Over	± 0.5
Angles			± 2°

Figure 8-7: SOM-Express Heat-Spreader Tolerances

8.8.3 Heat-Sink





General Dimension Tolerances (Unit : mm)			
0	—	30	± 0.2
31	—	60	± 0.3
61	—	100	± 0.4
101	and	Over	± 0.5
Angles			± 2°

Figure 8-8: Heatsink Dimensions

Table 8.2: Chemistry Ingredient & Temper Designation									
Mechanical Characteristics									
Alloy No.		Designation		Cutting Area Surface			Extension Rate		
6063		T5		Over 15kgf/mmxmm			7%		
Chemistry Ingredient & Temper Designation									
Value	Si	Fe	Cu	Mn	Cr	Mg	Zn	Ti	Flatness
SPECIFIED	0.4258	0.2037	0.0032	0.0059	0.0028	0.5147	0.0000	0.00263	<0.1mm

8.8.4 Thermal Pad

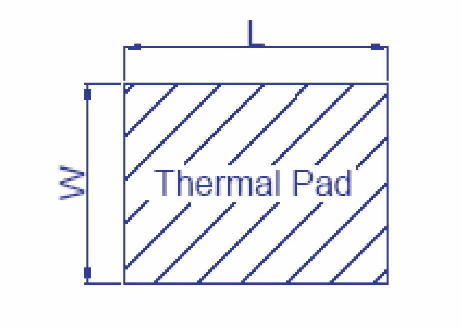


Figure 8-8: Thermal Pad

Table 8.3 Thermal Pad			
Item	**Specification**	**Brand**	**SIZE (mm)**
CPU	80GR-HM	FUJIPOLY SARCON	19.5*19.5*0.8
MCH	80GR-HM	FUJIPOLY SARCON	19.5*19.5*0.8
ICH	50GR-HM	FUJIPOLY SARCON	19.5*19.5*0.5

Data Sheet SARCON GR-Hm

SARCON GR-Hm

Highly-conformable, highly-compressible,
high-performance silicone polymer interface material.
Available thickness 0.3 to 3mm

Characteristics	Unit	0.3mm	0.5mm	0.8mm	1mm	1.25mm	1.5mm	2mm	2.5mm	3mm
Color	/	reddish gray	reddish gray	reddish gray	reddish gray	reddish gray	reddish gray	reddish gray	reddish gray	reddish gray
Thermal impedance	°Cin²/W	0.18	0.27	0.36	0.45	0.52	0.58	0.75	0.84	0.92
Thermal conductivity	W/mK	6	6	6	6	6	6	6	6	6
Dielectric strength	KV/mm	19	19	19	19	19	19	19	19	19
Dielectric breakdown	KV/mm	13	13	13	13	13	13	13	13	13
Volume resistivity	MΩ*m	10^5	10^5	10^5	10^5	10^5	10^5	10^5	10^5	10^5
Thickness	mm	0.3±0.1	0.5±0.1	0.8±0.1	1±0.2	1.25±0.2	1.5±0.2	2±0.3	2.5±0.3	3±0.3
Tensile strength	MPa	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3
Tear resistance	KN/m	1	1	1	1	1	1	1	1	1
Elongation	%	80	80	80	80	80	80	80	80	80
Specific gravity	/	3.2	3.2	3.2	3.2	3.2	3.2	3.2	3.2	3.2
Hardness	Shore 00	52	52	52	52	52	52	52	52	52
Pressure for 10% of compression	Kgf/in²	/	13.9	/	15.6	/	14.6	9.3	9.5	8.3
Pressure for 20% of compression	Kgf/in²	/	38.4	/	36.4	/	31.9	38.5	40.2	36.9
Pressure for 30% of compression	Kgf/in²	/	59.2	/	56.1	/	53.7	49.8	49.5	45.7
Pressure for 40% of compression	Kgf/in²	/	80.9	/	81.5	/	79.3	68.4	67.5	60.8
Pressure for 50% of compression	Kgf/in²	/	104.3	/	103.2	/	97.3	85.4	81.5	79.5
Sustain 50% of compression	Kgf/in²	/	76.6	/	74.9	/	68.8	54.2	50.3	42.5
UL flammability class	/	94 V-0	94 V-0	94 V-0	94 V-0	94 V-0	94 V-0	94 V-0	94 V-0	94 V-0
Operating temperature range	°C	-60 to +200	-60 to +200	-60 to +200	-60 to +200	-60 to +200	-60 to +200	-60 to +200	-60 to +200	-60 to +200

8.8.5 Screws

Table 8.4 Screws

Specification	Quantity
M2.5*6	5
M2.5*16	5

8.8.6 Fan

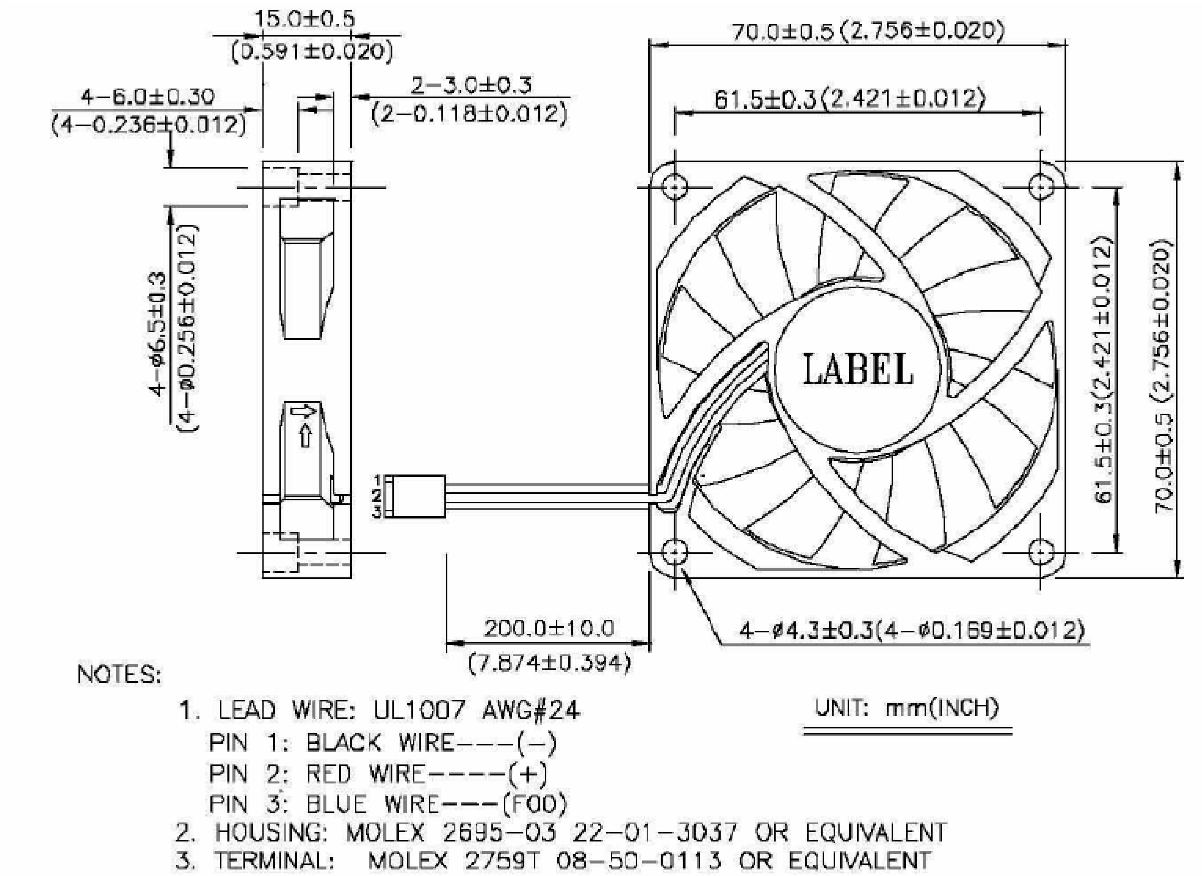
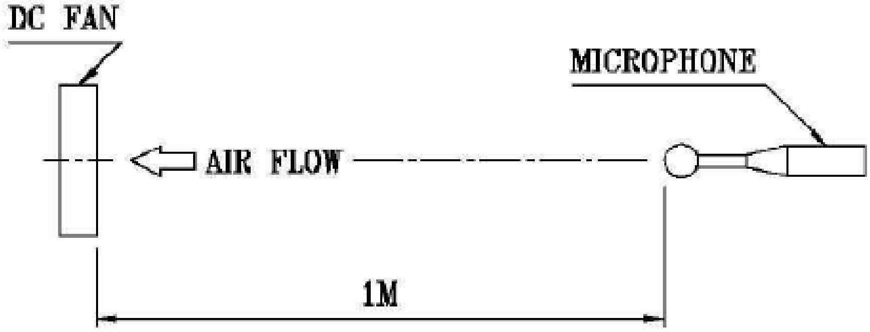


Figure 8-8: Fan

Table 8.5: Fan Characteristics

ITEM	DESCRIPTION
RATED VOLTAGE	12 VDC
OPERATION VOLTAGE	4.0 – 13.8 VDC
START VOLTAGE (ENVIRONMENT TEMPERATURE 25°C)	≤ 5.0 VDC.
INPUT CURRENT	0.26 (MAX. 0.45) A
INPUT POWER	3.12 (MAX. 5.40) W
SPEED	4300 R.P.M. (REF.)
MAX. AIR FLOW (AT ZERO STATIC PRESSURE)	1.063 (MIN. 0.957) M^3/MIN. 37.54 (MIN. 33.80) CFM
MAX. AIR PRESSURE (AT ZERO AIRFLOW)	5.33 (MIN. 4.32) mmH_2O 0.210 (MIN. 0.170) $inchH_2O$
ACOUSTICAL NOISE (AVG.)	38.5 (MAX. 42.5) dB-A
INSULATION TYPE	UL: CLASS A
INSULATION STRENGTH	10 MEG OHM MIN. AT 500 VDC (BETWEEN FRAME AND (+) TERMINAL)
DIELECTRIC STRENGTH	5 mA MAX. AT 500 VAC 60 Hz ONE MINUTE, (BETWEEN FRAME AND (+) TERMINAL)
EXTERNAL COVER	OPEN TYPE
LIFE EXPECTANCE	70,000 HOURS CONTINUOUS OPERATION AT 40 °C WITH 15 ~ 65 %RH.
ROTATION	CLOCKWISE VIEW FROM NAME PLATE SIDE
OVER CURRENT SHUT DOWN	THE CURRENT WILL SHUT DOWN WHEN LOCKING ROTOR.
LEAD WIRE	UL 1007 –F– AWG #24 BLACK WIRE NEGATIVE(–) RED WIRE POSITIVE(+) BLUE WIRE FREQUENCY(–FOO)

NOTES: 1. ALL READINGS ARE MEASURED AFTER STABLY WARMING UP THROUGH 10 MINUTES.
2. THE VALUES WRITTEN IN PARENS , ( ), ARE LIMITED SPEC.
3. ACOUSTICAL NOISE MEASURING CONDITION:



NOISE IS MEASURED AT RATED VOLTAGE IN FREE AIR IN ANECHOIC CHAMBER WITH B & K SOUND LEVEL METER WITH MICROPHONE AT A DISTANCE OF ONE METER FROM THE FAN INTAKE.